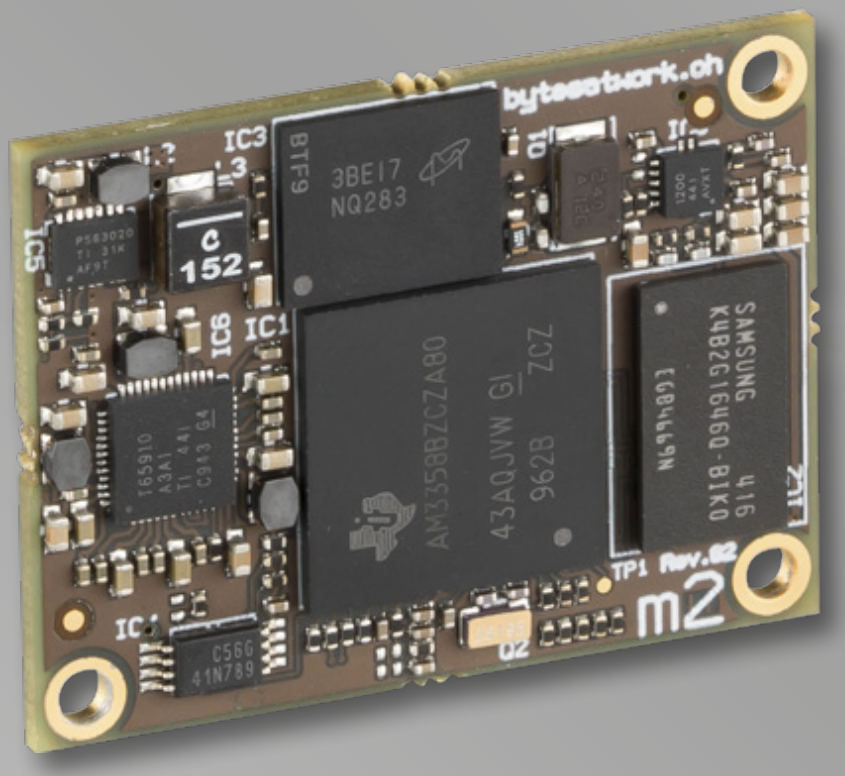
Datasheet

industrial computing module

byteENGINE AM335x

Ver. 0.5 – 18. 07 2019



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Imprint

> bytes at work AG
Technoparkstrasse 7
CH-8406 Winterthur
+41 52 213 79 79

> info@bytesatwork.ch
www.bytesatwork.io

Symbols and typographic conventions

These symbols represent important details or aspects for working with bytes at work AG-products.

NOTICE
Follow instructions. Acting against the procedure described can lead to malfunction.

LINK
Hyper- or Chapter-Link.

Table of Contents

1. Hardware Revisions

Hardware Revision	Marking on PCB	Release Date
1.0	m2 Rev.01	2013
2.0	m2 Rev.02	2015
4.0	m2 Rev.04	2017

2. Revisions history

2.1 Hardware revision 1.0

> 1.0 is the first version available for sales, end of life

2.2 Hardware revision 2.0

> New layout, for DDR3 RAM support up to 512MB

2.3 Hardware revision 4.0

> DDR3 RAM support up to 1GB

> Implementation of eMMC

> SPI-NOR flash (boot medium)

3. Overview

3.1 General Information

The byteENGINE AM335x is a high performance industrial oriented computing module. It allows a short time-to-market, while reducing development costs and substantial design risks.

The system on module (SOM) uses the Texas Instruments AM335x industrial applications processor family. The AM335x features a PowerVRTM SGX Graphics Accelerator Subsystem for 3D graphics acceleration.

The Programmable Real-Time Unit and Industrial Communication Subsystem (PRU-ICSS) allows independent operation from the ARM processor. PRU-ICSS enables real-time protocols such as EtherCAT, PROFINET, EtherNet/IP, PROFIBUS, Ethernet Powerlink and Sercos.

Scalable platform

> The AM335x Processor Family provides 6 PIN-compatible devices.

> 2 integrated PRU-ICSS deliver support for Ethercat-, Profibus and other Feldbus-Protocolls.

> The module byteENGINE AM335x is the perfect basis for innovative developments.

Expandable design

> The module provides a matching Linux-Kernel. As a result, the byteENGINE offers flexibility for almost any requirement.

> The free available open-source code allows reliable functionality and maximum extensibility.

3.2 Technical Data

Feature		Details
CPU	Architecture	ARM® Cortex™ -A8
	CPU	Texas Instruments - see Chart for CPU-Models: „3.4 Overview of AM335x Processors“
	Frequency (max)	1000 MHz
	Floating Point	YES (NEON™, SIMD & VFP)
	PRU	Up to two (200 MHz)
Memory	SDRAM	64 MB - 1 GB DDR3
	NAND or eMMC	256 MB NAND / 4 GB eMMC
	SPI-NOR	16 MB (boot medium, eMMC variants only)
	EEPROM	32 KB (containing HW configuration)
Ethernet	Speed	2x 10/100/1.000 (Mbit/s)
Multimedia	Video	Parallel RGB 24bit
	2D/3D Graphics	Power VR™ SGX530 (AM3359, AM3358 and AM3354 only)
	Touchscreen	Supported
	Audio	Yes
Expansion	SD/MMC/SDIO	3
Serial	McASP	2
	SPI	2
	I^2C	3
	UART	6
	CAN	2
USB	OTG	2 HS (2.0)
Miscellaneous	Watchdog Timers	1
	GPMC	Yes (Full Pinout)
	JTAG	Yes
	Serial Console	1
	GPIO	4x 32 GPIOS
	PWM / ECAP / QEP	3
	Boot Mode	Selectable with Strapping Pins on Baseboard
Mechanical Information	Input Voltage	3 - 5 V
	Power Consumption	~2 W
	Dimensions	30 x 40 x 5 mm
	Operational Temperature	-40 to +85 °C
	Connector	2x 100 pin
Operating System	Linux (yocto)	Yes meta-bytesatwork available on github: follow LINK

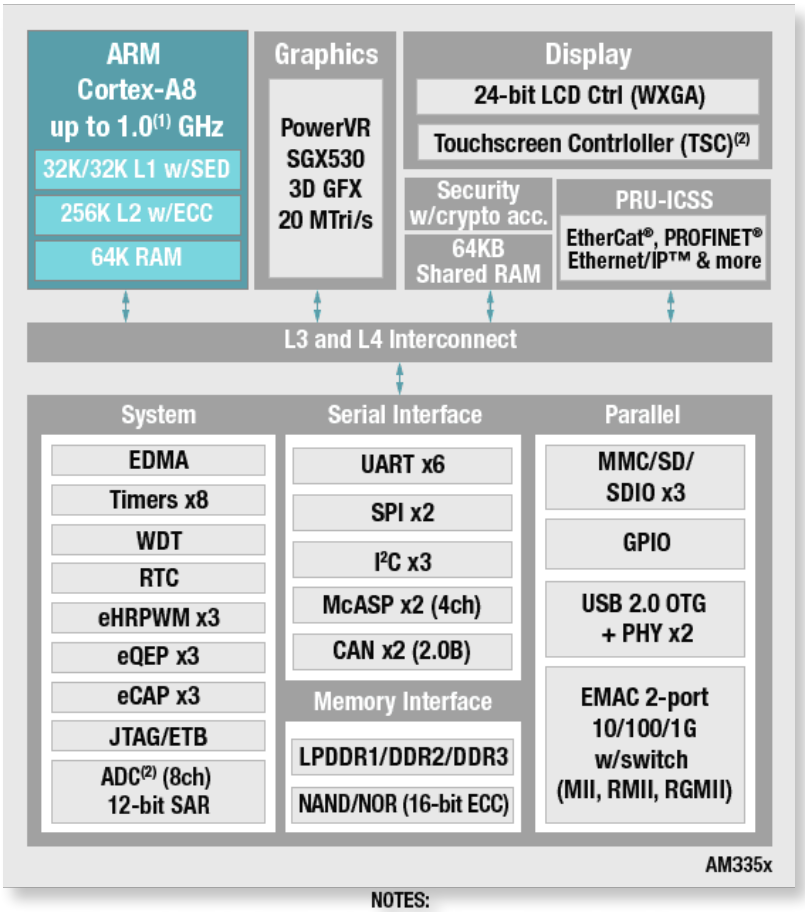
3.3 AM335x block diagram

TI's Sitara™ AM335x Processor is based on highly-optimized ARM® Cortex®-A8 core for performance and power efficiency. The AM335x Cortex-A8-based processor can meet the requirements for power optimized systems with a power budget of less than 1Watt.

The AM335x microprocessor contains the subsystems shown in the Functional Block Diagram:

Key Features of AM335x

- ARM Cortex-A8 processor, scalable from 300MHz to 1GHz
- 3D graphics option for enhanced user interface
- Dual core PRU-ICSS for industrial Ethernet protocols and position feedback control
- Robust hardware enablement for differentiated peripherals: LCD Controller, CAN, Gigabit EMAC, 2x USB w/PHY, touch screen control, integrated industrial protocols
- 2000 MIPS and a power consumption of less than 2 Watt is Green IT by definition
- The scalable memory (128MB up to 1GB) can be operated from -40° up to +85° Celsius



NOTES:
(1) >800MHz available on 15x15 package,13x13 supports up to 600MHz
(2) Use of TSC will limit available ADC channels
SED: Single error detection/parity

3.4 Overview of AM335x Processors

AM335x Processors	AM3359	AM3358	AM3357	AM3356	AM3354	AM3352
ARM Cortex-A8 MHz	800	600/ 800/ 1000	300/ 600/ 800	300/ 600/ 800	600/ 800/ 1000	300/ 600/ 800/ 1000
3D graphics Acceleration	☑	☑	⊗	⊗	☑	⊗
PRU-ICSS for industrial communication[1]	Dual core PRU + all protocols[3]	Dual core PRU + standard protocols[2]	Dual core PRU + all protocols[3]	Dual core PRU + standard protocols[2]	⊗	⊗
CAN	2	2	2	2	2	2
Package 15x15 / 0.8mm	☑	☑	☑	☑	☑	☑
Software		Software and pin-for-pin compatible across devices				

[1] PRU-ICSS is a programmable real-time subsystem for industrial communication protocols.
[2] Standard protocols for AM335x processors include protocols such as Ethernet/IP, PROFINET™ RT/IRT, PROFIBUS™, Sercos III, and more.
[3] All Protocols for AM335x processors include standard protocols plus EtherCAT™ and POWERLINK.

LINK:
Texas Instruments Sitara™ AM335x Processors

3.5 Decision guidance byteENGINE AM335x

The following three steps help identifying the suitable TI Sitara™ AM335x Processor for the specific customer application.

> Step 1: The choice of needed CPU-Speed.

- **CPU-Speed: 300 up to 1.000 MHz**
  for details see **„3.4 Overview of AM335x Processors“**

> Step 2: Which Memory-Type is suitable?

- **eMMC**
- **NAND**

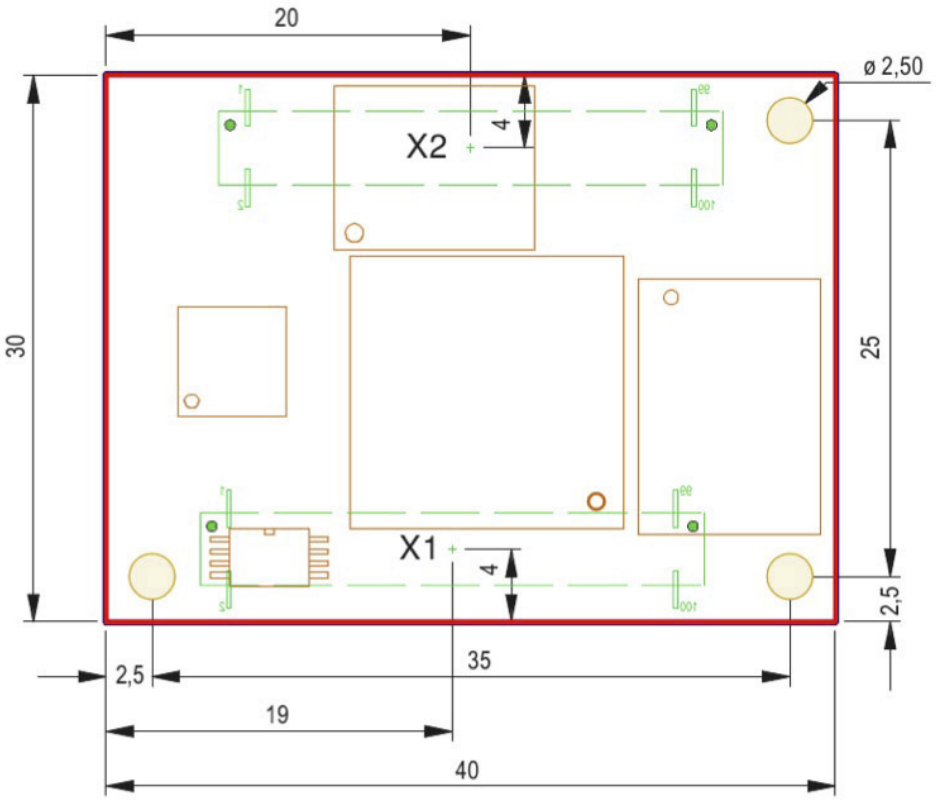
> Step 3: The choice of needed RAM capacity.

- **Min: 128 MB**
- **Max: 1 GB**

3.6 Dimensions of AM335x

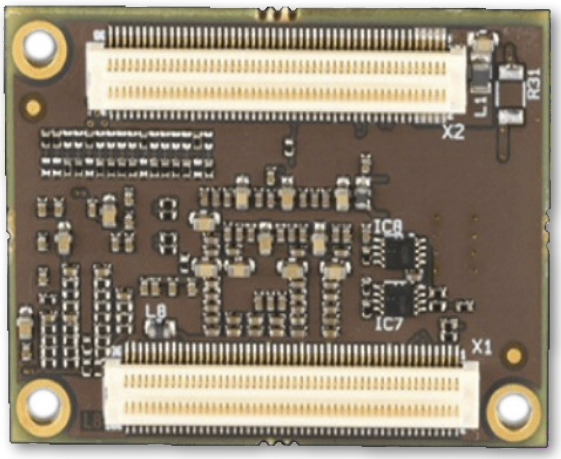
The following illustration shows all important dimensions for mounting and installation of the industrial computing module byteENGINE AM335x.

> All dimensions are indicated in millimetres (mm).



3.7 AM335x connectors layout

The AM335x is connected to the carrier board with 200 pins on two module connectors. The following picture shows the location of the connectors on the bottom side of the byteENGINE.

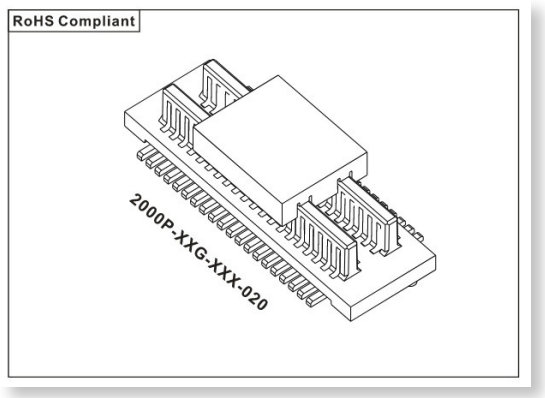


LINK:
Schematic of the connectors X1 and X2

NOTICE
The module is held in the connectors with a considerable retention force. To avoid damaging the connectors while removing the module, the use of an extraction tool is highly recommended.

3.8 Connectors - Neltron 2001S-100G-270-020

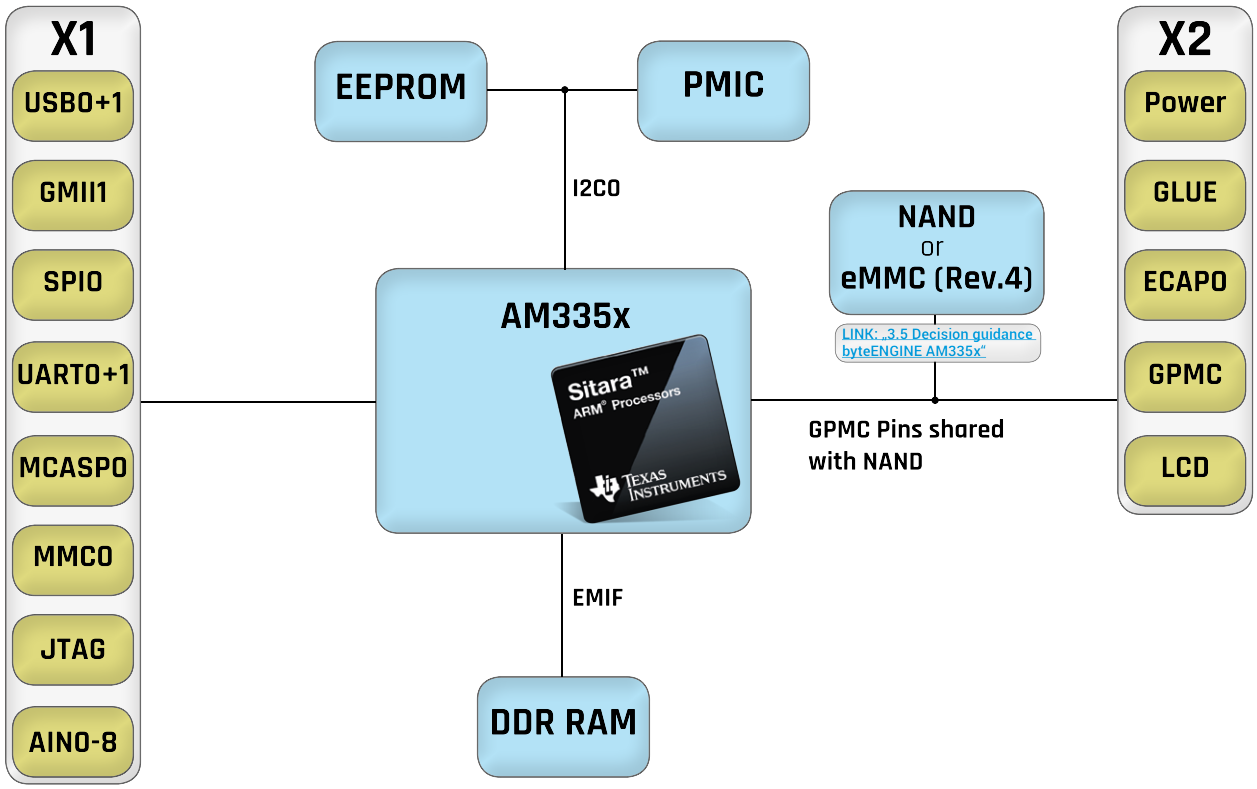
The byteENGINE uses three Neltron 0,5mm Board to Board Plug connectors.
For more specific information about the connectors used, please visit:



LINK:
Datasheet of Neltron 0,5mm Connectors

3.9 byteENGINE AM335x Connectors Overview

The following illustration shows the „Default-Configuration" of the byteENGINE AM335x. The function of the components shown in blue squares cannot be changed. The yellow squares show the module connectors X1 and X2. The functions of X1 and X2 can be adapted and each connector module serves multiple functions. The detailed pinout-functions are shown in chapter „4. Pinouts"



3.10 PinMux Tool - configuring the AM335x Processor

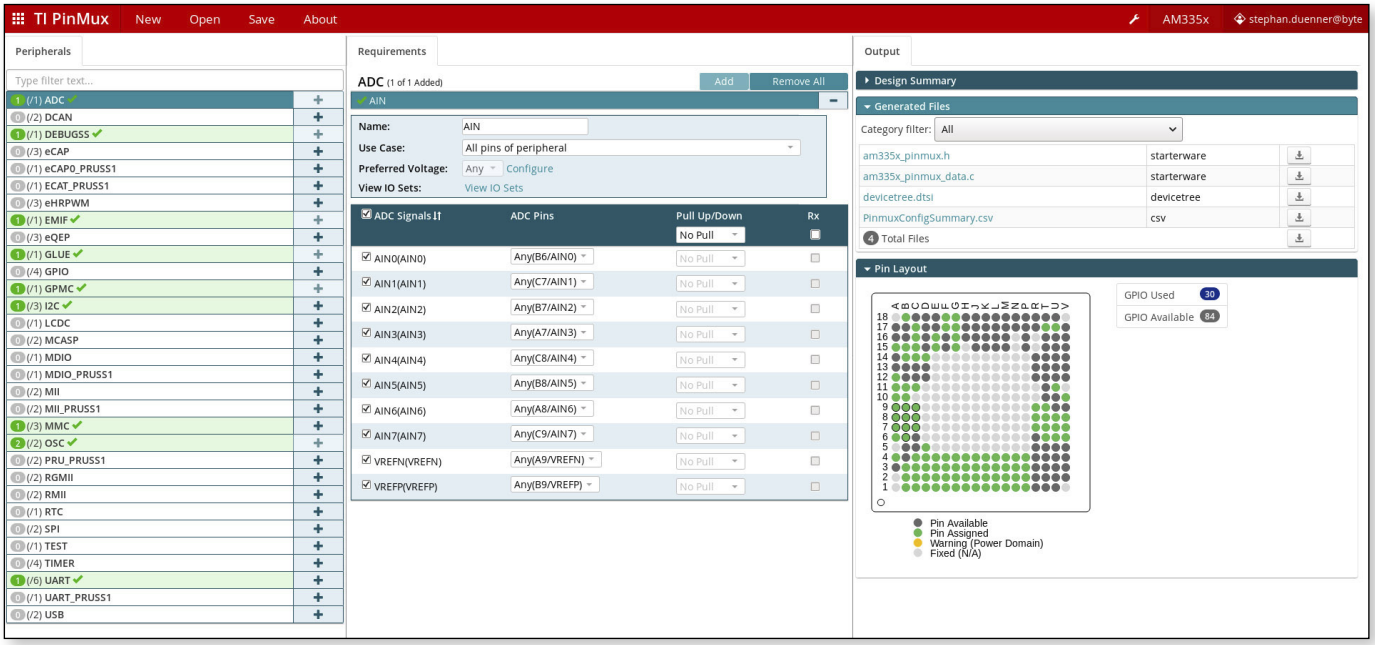
The Pin MUX Utility is a software tool which provides a Graphical User Interface for configuring pin multiplexing settings, resolving conflicts and specifying I/O cell characteristics for TI MPUs. Results are output as C header/code files that can be imported into software development kits (SDKs) or used to configure customer's custom software.

Version 4 of the Pin MUX Utility adds the capability of automatically selecting a mux configuration that satisfies the entered requirements.

NOTICE
Follow the Link to Pinmux Tool.
You need to LOG-IN first.
Then choose the AM335x Processor.
See illustration for details.

LINK:
Pinmux Tool

LINK:
Prepared Pinmux File



4. Pinouts

The multiple pin configurations must be taken note when using processor signals.
The pins of the module connectors are described in detail in the following tables.

4.1 Carrier board connectors X1

Con	Pin	Signal_Name	Available Modes on Pin								Note
			0	1	2	3	4	5	6	7	
X1	1	GND									
X1	2	GND									
X1	3	SYS_nWarmreset									
X1	4	nNMI	nNMI,								
X1	5	nRESETIN_OUT	nRESETIN_OUT								
X1	6	GND									
X1	7	USB0_DRVVBUS	USB0_DRVVBUS							gpio0[18]	
X1	8	USB1_DRVVBUS	USB1_DRVVBUS							gpio3[13]	
X1	9	USB0_DM	USB0_DM,								
X1	10	USB1_DM	USB1_DM								
X1	11	USB0_DP	USB0_DP								
X1	12	USB1_DP	USB1_DP								
X1	13	USB0_VBUS	USB0_VBUS								
X1	14	USB1_VBUS	USB1_VBUS								
X1	15	USB0_ID	USB0_ID,								
X1	16	USB1_ID	USB1_ID,								
X1	17	GND									
X1	18	GND									
X1	19	mdio_clk	mdio_clk	timer5	uart5_txd	uart3_rtsn	mmc0_sdwp	mmc1_clk	mmc2_clk	gpio0[1]	
X1	20	mdio_data	mdio_data	timer6	uart5_rxd	uart3_ctsn	mmc0_sdcd	mmc1_cmd	mmc2_cmd	gpio0[0]	
X1	21	GND									
X1	22	GND									
X1	23	gmii1_txd0	gmii1_txd0	rmii1_txd0	rgmii1_td0	mcasp1_ axr2	mcasp1_aclkr	eQEP0B_in	mmc1_clk	gpio0[28]	
X1	24	gmii1_rxd0	gmii1_rxd0	rmii1_rxd0	rgmii1_rd0	mcasp1_ah- clkx	mcasp1_ah- clkr	mcasp1_aclkr	mcasp0_ axr3	gpio2[21]	
X1	25	gmii1_txd1	gmii1_txd1	rmii1_txd1	rgmii1_td1	mcasp1_fsr	mcasp1_axr1	eQEP0A_in	mmc1_cmd	gpio0[21]	
X1	26	gmii1_rxd1	gmii1_rxd1	rmii1_rxd1	rgmii1_rd1	mcasp1_ axr3	mcasp1_fsr	eQEP0_strobe	mmc2_clk	gpio2[20]	
X1	27	gmii1_txd2	gmii1_txd2	dcan0_rx	rgmii1_td2	uart4_txd	mcasp1_axr0	mmc2_dat2	mcasp0_ah- clkx	gpio0[17]	
X1	28	gmii1_rxd2	gmii1_rxd2	uart3_txd	rgmii1_rd2	mmc0_dat4	mmc1_dat3	uart1_rin	mcasp0_ axr1	gpio2[19]	
X1	29	gmii1_txd3	gmii1_txd3	dcan0_tx	rgmii1_td3	uart4_rxd	mcasp1_fsx	mmc2_dat1	mcasp0_fsr	gpio0[16]	
X1	30	gmii1_rxd3	gmii1_rxd3	uart3_rxd	rgmii1_rd3	mmc0_dat5	mmc1_dat2	uart1_dtrn	mcasp0_ axr0	gpio2[18]	
X1	31	gmii1_txclk	gmii1_txclk	uart2_rxd	rgmii1_tclk	mmc0_dat7	mmc1_dat0	uart1_dcdn	mcasp0_ aclkx	gpio3[9]	

Follow link for explanation
„4.2.1 Yellow and Pink Marked X1- and X2-Connectors“

Con	Pin	Signal_Name	Available Modes on Pin								Note
			0	1	2	3	4	5	6	7	
X1	32	gmii1_rxclk	gmii1_rxclk	uart2_txd	rgmii1_rclk	mmc0_dat6	mmc1_dat1	uart1_dsrn	mcasp0_fsx	gpio3[10]	
X1	33	gmii1_txen	gmii1_txen	rmii1_txen	rgmii1_tctl	timer4	mcasp1_axr0	eQEP0_index	mmc2_cmd	gpio3[3]	
X1	34	gmii1_rxer	gmii1_rxer	rmii1_rxer	spi1_d1	I2C1_SCL	mcasp1_fsx	uart5_rtsn	uart2_txd	gpio3[2]	
X1	35	gmii1_col	gmii1_col	rmii2_refclk	spi1_sclk	uart5_rxd	mcasp1_axr2	mmc2_dat3	mcasp0_axr2	gpio3[0]	
X1	36	gmii1_rxdv	gmii1_rxdv	lcd_memory_clk	rgmii1_rctl	uart5_txd	mcasp1_aclkx	mmc2_dat0	mcasp0_aclkr	gpio3[4]	
X1	37	gmii1_crs	gmii1_crs	rmii1_crs_dv	spi1_d0	I2C1_SDA	mcasp1_aclkx	uart5_ctsn	uart2_rxd	gpio3[1]	
X1	38	rmii1_refclk	rmii1_refclk	xdma_event_intr2	spi1_cs0	uart5_txd	mcasp1_axr3	mmc0_pow	mcasp1_ahclkx	gpio0[29]	
X1	39	GND									
X1	40	GND									
X1	41	spi0_cs0	spi0_cs0	mmc2_sdwp	I2C1_SCL	ehrpwm0_synci	pr1_uart0_txd	pr1_edio_data_in1	pr1_edio_data_out1	gpio0[5]	SPI NOR Bridge to GPMC_WAIT0
X1	42	spi0_d0	spi0_d0	uart2_txd	I2C2_SCL	ehrpwm0B	pr1_uart0_rts_n	pr1_edio_latch_in	EMU3	gpio0[3]	SPI NOR must be SPI
X1	43	spi0_cs1	spi0_cs1	uart3_rxd	eCAP1_in_PWM1_out	mmc0_pow	xdma_event_intr2	mmc0_sdcd	EMU4	gpio0[6]	
X1	44	spi0_d1	spi0_d1	mmc1_sdwp	I2C1_SDA	Ehrpwm0_tripzone_input	pr1_uart0_rxd	pr1_edio_data_in0	pr1_edio_data_out0	gpio0[4]	SPI NOR must be SPI
X1	45	spi0_sclk	spi0_sclk	uart2_rxd	I2C2_SDA	ehrpwm0A	pr1_uart0_cts_n	pr1_edio_sof	EMU2	gpio0[2]	SPI NOR must be SPI
X1	46	GND									
X1	47	GND									
X1	48	GND									
X1	49	uart0_txd	uart0_txd	spi1_cs1	dcan0_rx	I2C2_SCL	eCAP1_in_PWM1_out	pr1_pru1_pru_r30[15]	pr1_pru1_pru_r31[15]	gpio1[11]	
X1	50	uart1_txd	uart1_txd	mmc2_sdwp	dcan1_rx	I2C1_SCL		pr1_uart0_txd	pr1_pru0_pru_r31[16]	gpio0[15]	
X1	51	uart0_rxd	uart0_rxd	spi1_cs0	dcan0_tx	I2C2_SDA	eCAP2_in_PWM2_out	pr1_pru1_pru_r30[14]	pr1_pru1_pru_r31[14]	gpio1[10]	
X1	52	uart1_rxd	uart1_rxd	mmc1_sdwp	dcan1_tx	I2C1_SDA		pr1_uart0_rxd	pr1_pru1_pru_r31[16]	gpio0[14]	
X1	53	uart0_ctsn	uart0_ctsn	uart4_rxd	dcan1_tx	I2C1_SDA	spi1_d0	timer7	pr1_edc_sync0_out	gpio1[8]	
X1	54	uart1_ctsn	uart1_ctsn	timer6	dcan0_tx	I2C2_SDA	spi1_cs0	pr1_uart0_cts_n	pr1_edc_latch0_in	gpio0[12]	
X1	55	uart0_rtsn	uart0_rtsn	uart4_txd	dcan1_rx	I2C1_SCL	spi1_d1	spi1_cs0	pr1_edc_sync1_out	gpio1[9]	
X1	56	uart1_rtsn	uart1_rtsn	timer5	dcan0_rx	I2C2_SCL	spi1_cs1	pr1_uart0_rts_n	pr1_edc_latch1_in	gpio0[13]	
X1	57	GND									
X1	58	GND									
X1	59	mcasp0_aclkx	mcasp0_aclkx	ehrpwm0A		spi1_sclk	mmc0_sdcd	pr1_pru0_pru_r30[0]	pr1_pru0_pru_r31[0]	gpio3[14]	
X1	60	mcasp0_fsx	mcasp0_fsx	ehrpwm0B		spi1_d0	mmc1_sdcd	pr1_pru0_pru_r30[1]	pr1_pru0_pru_r31[1]	gpio3[15]	
X1	61	mcasp0_ahclkx	mcasp0_ahclkx	eQEP0_strobe	mcasp0_axr3	mcasp1_axr1	EMU4	pr1_pru0_pru_r30[7]	pr1_pru0_pru_r31[7]	gpio3[21]	
X1	62	mcasp0_fsr	mcasp0_fsr	eQEP0B_in	mcasp0_axr3	mcasp1_fsx	EMU2	pr1_pru0_pru_r30[5]	pr1_pru0_pru_r31[5]	gpio3[19]	

4.1 Carrier board connectors X1

Con	Pin	Signal_Name	Available Modes on Pin								Note
			0	1	2	3	4	5	6	7	
X1	63	mcasp0_aclkr	mcasp0_aclkr	eQEP0A_in	mcasp0_axr2	mcasp1_aclkx	mmc0_sdwp	pr1_pru0_pru_r30[4]	pr1_pru0_pru_r31[4]	gpio3[18]	
X1	64	mcasp0_axr0	mcasp0_axr0	ehrpwm0_tripzone_input		spi1_d1	mmc2_sdcd	pr1_pru0_pru_r30[2]	pr1_pru0_pru_r31[2]	gpio3[16]	
X1	65	mcasp0_ahclkr	mcasp0_ahclkr	ehrpwm0_synci	mcasp0_axr2	spi1_cs0	eCAP2_in_PWM2_out	pr1_pru0_pru_r30[3]	pr1_pru0_pru_r31[3]	gpio3[17]	
X1	66	mcasp0_axr1	mcasp0_axr1	eQEP0_index		mcasp1_axr0	EMU3	pr1_pru0_pru_r30[6]	pr1_pru0_pru_r31[6]	gpio3[20]	
X1	67	GND									
X1	68	GND									
X1	69	mmc0_dat0	mmc0_dat0	gpmc_a23	uart5_rtsn	uart3_txd	uart1_rin	pr1_pru0_pru_r30[11]	pr1_pru0_pru_r31[11]	gpio2[29]	
X1	70	mmc0_cmd	mmc0_cmd	gpmc_a25	uart3_rtsn	uart2_txd	dcan1_rx	pr1_pru0_pru_r30[13]	pr1_pru0_pru_r31[13]	gpio2[31]	
X1	71	mmc0_dat1	mmc0_dat1	gpmc_a22	uart5_ctsn	uart3_rxd	uart1_dtrn	pr1_pru0_pru_r30[10]	pr1_pru0_pru_r31[10]	gpio2[28]	
X1	72	mmc0_clk	mmc0_clk	gpmc_a24	uart3_ctsn	uart2_rxd	dcan1_tx	pr1_pru0_pru_r30[12]	pr1_pru0_pru_r31[12]	gpio2[30]	
X1	73	mmc0_dat2	mmc0_dat2	gpmc_a21	uart4_rtsn	timer6	uart1_dsrn	pr1_pru0_pru_r30[9]	pr1_pru0_pru_r31[9]	gpio2[27]	
X1	74	VMMC									
X1	75	mmc0_dat3	mmc0_dat3	gpmc_a20	uart4_ctsn	timer5	uart1_dcdn	pr1_pru0_pru_r30[8]	pr1_pru0_pru_r31[8]	gpio2[26]	
X1	76	VMMC									
X1	77	GND									
X1	78	GND									
X1	79	nTRST	nTRST								
X1	80	TDO	TDO								
X1	81	TCK	TCK								
X1	82	TDI	TDI								
X1	83	TMS	TMS								
X1	84	EMU0	EMU0							gpio3[7]	
X1	85	AGND									
X1	86	EMU1	EMU1							gpio3[8]	
X1	87	AGND									
X1	88	GND									
X1	89	AIN0	AIN0								
X1	90	AIN1	AIN1								
X1	91	AIN2	AIN2								
X1	92	AIN3	AIN3								
X1	93	AIN4	AIN4								
X1	94	AIN5	AIN5								
X1	95	AIN6	AIN6								
X1	96	AIN7	AIN7								
X1	97	GND									
X1	98	GND									
X1	99	GND									
X1	100	GND									

4.2 Carrier board connectors X2

Con	Pin	Signal Name	Available Modes on Pin								Note
			0	1	2	3	4	5	6	7	
X2	1	VBAT									
X2	2	VBAT									
X2	3	VBAT									
X2	4	VBAT									
X2	5	VBAT									
X2	6	VBAT									
X2	7	VBAT									
X2	8	VBAT									
X2	9	VBAT									
X2	10	VBAT									
X2	11	GND									
X2	12	GND									
X2	13	GND									
X2	14	GND									
X2	15	GND									
X2	16	GND									
X2	17	Sleep (PMIC)									
X2	18	eCAP0_in_PWM0_out	eCAP0_in_PWM0_out	uart3_txd	spi1_cs1	pr1_ecap0_ecap_capin_apwm_o	spi1_sclk	mmc0_sdwp	xdma_event_intr2	gpio0[7]	
X2	19	PWRON (PMIC)									
X2	20	EXT_WAKEUP	EXT_WAKEUP								
X2	21	Vbackup (PMIC)									
X2	22	GND									
X2	23	GND									
X2	24	GND									
X2	25	n.c.									
X2	26	xdma_event_intr0	xdma_event_intr0		timer4	clkout1	spi1_cs1	pr1_pru1_pru_r31[16]	EMU2	gpio0[19]	
X2	27	n.c.									
X2	28	xdma_event_intr1	xdma_event_intr1		tclkin	clkout2	timer7	pr1_pru0_pru_r31[16]	EMU3	gpio0[20]	
X2	29	VREFP	VREFP,								
X2	30	n.c.									
X2	31	VREFN	VREFN,								
X2	32	n.c.									
X2	33	GND									
X2	34	GND									
X2	35	gpmc_wait0	gpmc_wait0	gmii2_crs	gpmc_csn4	rmii2_crs_dv	mmc1_sdcd	pr1_mii1_col	uart4_rxd	gpio0[30]	NAND
X2	36	gpmc_be1n	gpmc_be1n	gmii2_col	gpmc_csn6	mmc2_dat3	gpmc_dir	pr1_mii1_rxlink	mcasp0_aclkr	gpio1[28]	
X2	37	gpmc_wpn	gpmc_wpn	gmii2_rxer	gpmc_csn5	rmii2_rxer	mmc2_sdcd	pr1_mii1_txen	uart4_txd	gpio0[31]	NAND
X2	38	gpmc_be0n_cle	gpmc_be0n_cle		timer5					gpio2[5]	NAND
X2	39	gpmc_advn_ale	gpmc_advn_ale		timer4					gpio2[2]	NAND
X2	40	gpmc_csn3	gpmc_csn3	gpmc_a3	rmii2_crs_dv	mmc2_cmd	pr1_mii0_crs	pr1_mdio_data	EMU4	gpio2[0]	
X2	41	gpmc_oen_ren	gpmc_oen_ren		timer7					gpio2[3]	NAND
X2	42	gpmc_csn2	gpmc_csn2	gpmc_be1n	mmc1_cmd	pr1_edio_data_in7	pr1_edio_data_out7	pr1_pru1_pru_r30[13]	pr1_pru1_pru_r31[13]	gpio1[31]	eMMC Bridge to GPMC_Wpn
X2	43	gpmc_wen	gpmc_wen	timer6	gpio2[4]						NAND
X2	44	gpmc_csn1	gpmc_csn1	gpmc_clk	mmc1_clk	pr1_edio_data_in6	pr1_edio_data_out6	pr1_pru1_pru_r30[12]	pr1_pru1_pru_r31[12]	gpio1[30]	eMMC Bridge to GPMC_WAIT0

4.2 Carrier board connectors X2

Follow link for explanation
„4.2.1 Yellow and Pink Marked X1- and X2-Connectors“

Con	Pin	Signal_Name	Available Modes on Pin								Note
			0	1	2	3	4	5	6	7	
X2	45	gpmc_clk	gpmc_clk	lcd_memory_clk	gpmc_wait1	mmc2_clk	pr1_mii1_crs	pr1_mdio_mdclk	mcasp0_fsr	gpio2[1]	
X2	46	gpmc_csn0	gpmc_csn0							gpio1[29]	NAND
X2	47	gpmc_ad14	gpmc_ad14	lcd_data17	mmc1_dat6	mmc2_dat2	eQEP2_index	pr1_mii0_txd0	pr1_pru0_pru_r31[14]	gpio1[14]	
X2	48	gpmc_ad15	gpmc_ad15	lcd_data16	mmc1_dat7	mmc2_dat3	eQEP2_strobe	pr1_ecap0_ecap_capin_apwm_o	pr1_pru0_pru_r31[15]	gpio1[15]	
X2	49	gpmc_ad12	gpmc_ad12	lcd_data19	mmc1_dat4	mmc2_dat0	eQEP2A_in	pr1_mii0_txd2	pr1_pru0_pru_r30[14]	gpio1[12]	
X2	50	gpmc_ad13	gpmc_ad13	lcd_data18	mmc1_dat5	mmc2_dat1	eQEP2B_in	pr1_mii0_txd1	pr1_pru0_pru_r30[15]	gpio1[13]	
X2	51	gpmc_ad10	gpmc_ad10	lcd_data21	mmc1_dat2	mmc2_dat6	ehrpwm2_tripzone_input	pr1_mii0_txen		gpio0[26]	
X2	52	gpmc_ad11	gpmc_ad11	lcd_data20	mmc1_dat3	mmc2_dat7	ehrpwm0_synco	pr1_mii0_txd3		gpio0[27]	
X2	53	gpmc_ad8	gpmc_ad8	lcd_data23	mmc1_dat0	mmc2_dat4	ehrpwm2A	pr1_mii_mt0_clk		gpio0[22]	
X2	54	gpmc_ad9	gpmc_ad9	lcd_data22	mmc1_dat1	mmc2_dat5	ehrpwm2B	pr1_mii0_col		gpio0[23]	
X2	55	gpmc_ad6	gpmc_ad6	mmc1_dat6						gpio1[6]	eMMC and NAND
X2	56	gpmc_ad7	gpmc_ad7	mmc1_dat7						gpio1[7]	
X2	57	gpmc_ad4	gpmc_ad4	mmc1_dat4						gpio1[4]	
X2	58	gpmc_ad5	gpmc_ad5	mmc1_dat5						gpio1[5]	
X2	59	gpmc_ad2	gpmc_ad2	mmc1_dat2						gpio1[2]	
X2	60	gpmc_ad3	gpmc_ad3	mmc1_dat3						gpio1[3]	
X2	61	gpmc_ad0	gpmc_ad0	mmc1_dat0						gpio1[0]	
X2	62	gpmc_ad1	gpmc_ad1	mmc1_dat1						gpio1[1]	
X2	63	gpmc_a10	gpmc_a10	gmii2_rxd1	rgmii2_rd1	rmii2_rxd1	gpmc_a26	pr1_mii1_rxdv	mcasp0_axr0	gpio1[26]	
X2	64	gpmc_a11	gpmc_a11	gmii2_rxd0	rgmii2_rd0	rmii2_rxd0	gpmc_a27	pr1_mii1_rxer	mcasp0_axr1	gpio1[27]	
X2	65	gpmc_a8	gpmc_a8	gmii2_rxd3	rgmii2_rd3	mmc2_dat6	gpmc_a24	pr1_mii1_rxd0	mcasp0_aclkx	gpio1[24]	
X2	66	gpmc_a9	gpmc_a9	gmii2_rxd2	rgmii2_rd2	rmii2_crs_dv	gpmc_a25	pr1_mii_mr1_clk	mcasp0_fsx	gpio1[25]	
X2	67	gpmc_a6	gpmc_a6	gmii2_txclk	rgmii2_tclk	mmc2_dat4	gpmc_a22	pr1_mii1_rxd2	eQEP1_index	gpio1[22]	
X2	68	gpmc_a7	gpmc_a7	gmii2_rxclk	rgmii2_rclk	mmc2_dat5	gpmc_a23	pr1_mii1_rxd1	eQEP1_strobe	gpio1[23]	
X2	69	gpmc_a4	gpmc_a4	gmii2_txd1	rgmii2_td1	rmii2_txd1	gpmc_a20	pr1_mii1_txd0	eQEP1A_in	gpio1[20]	
X2	70	gpmc_a5	gpmc_a5	gmii2_txd0	rgmii2_td0	rmii2_txd0	gpmc_a21	pr1_mii1_rxd3	eQEP1B_in	gpio1[21]	
X2	71	gpmc_a2	gpmc_a2	gmii2_txd3	rgmii2_td3	mmc2_dat1	gpmc_a18	pr1_mii1_txd2	ehrpwm1A	gpio1[18]	
X2	72	gpmc_a3	gpmc_a3	gmii2_txd2	rgmii2_td2	mmc2_dat2	gpmc_a19	pr1_mii1_txd1	ehrpwm1B	gpio1[19]	
X2	73	gpmc_a0	gpmc_a0	gmii2_txen	rgmii2_tctl	rmii2_txen	gpmc_a16	pr1_mii_mt1_clk	ehrpwm1_tripzone_input	gpio1[16]	
X2	74	gpmc_a1	gpmc_a1	gmii2_rxdv	rgmii2_rctl	mmc2_dat0	gpmc_a17	pr1_mii1_txd3	ehrpwm0_synco	gpio1[17]	
X2	75	GND									
X2	76	GND									
X2	77	lcd_data14	lcd_data14	gpmc_a18	eQEP1_index	mcasp0_axr1	uart5_rxd	pr1_mii_mr0_clk	uart5_ctsn	gpio0[10]	
X2	78	lcd_data15	lcd_data15	gpmc_a19	eQEP1_strobe	mcasp0_ahclkx	mcasp0_axr3	pr1_mii0_rxdv	uart5_rtsn	gpio0[11]	

4.2 Carrier board connectors X2

Con	Pin	Signal_Name	Available Modes on Pin								Note
			0	1	2	3	4	5	6	7	
X2	79	lcd_data12	lcd_data12	gpmc_a16	eQEP1A_in	mcasp0_aclkr	mcasp0_axr2	pr1_mii0_rxlink	uart4_ctsn	gpio0[8]	
X2	80	lcd_data13	lcd_data13	gpmc_a17	eQEP1B_in	mcasp0_fsr	mcasp0_axr3	pr1_mii0_rxer	uart4_rtsn	gpio0[9]	
X2	81	lcd_data10	lcd_data10	gpmc_a14	ehrpwm1A	mcasp0_axr0	pr1_mii0_rxd1	uart3_ctsn	gpio2[16]		
X2	82	lcd_data11	lcd_data11	gpmc_a15	ehrpwm1B	mcasp0_ahclkr	mcasp0_axr2	pr1_mii0_rxd0	uart3_rtsn	gpio2[17]	
X2	83	lcd_data8	lcd_data8	gpmc_a12	ehrpwm1_tripzone_input	mcasp0_aclkx	uart5_txd	pr1_mii0_rxd3	uart2_ctsn	gpio2[14]	
X2	84	lcd_data9	lcd_data9	gpmc_a13	ehrpwm0_synco	mcasp0_fsx	uart5_rxd	pr1_mii0_rxd2	uart2_rtsn	gpio2[15]	
X2	85	lcd_data6	lcd_data6	gpmc_a6	pr1_edio_data_in6	eQEP2_index	pr1_edio_data_out6	pr1_pru1_pru_r30[6]	pr1_pru1_pru_r31[6]	gpio2[12]	
X2	86	lcd_data7	lcd_data7	gpmc_a7	pr1_edio_data_in7	eQEP2_strobe	pr1_edio_data_out7	pr1_pru1_pru_r30[7]	pr1_pru1_pru_r31[7]	gpio2[13]	
X2	87	lcd_data4	lcd_data4	gpmc_a4	pr1_mii0_txd1	eQEP2A_in		pr1_pru1_pru_r30[4]	pr1_pru1_pru_r31[4]	gpio2[10]	
X2	88	lcd_data5	lcd_data5	gpmc_a5	pr1_mii0_txd0	eQEP2B_in		pr1_pru1_pru_r30[5]	pr1_pru1_pru_r31[5]	gpio2[11]	
X2	89	lcd_data2	lcd_data2	gpmc_a2	pr1_mii0_txd3	ehrpwm2_tripzone_input		pr1_pru1_pru_r30[2]	pr1_pru1_pru_r31[2]	gpio2[8]	
X2	90	lcd_data3	lcd_data3	gpmc_a3	pr1_mii0_txd2	ehrpwm0_synco		pr1_pru1_pru_r30[3]	pr1_pru1_pru_r31[3]	gpio2[9]	
X2	91	lcd_data0	lcd_data0	gpmc_a0	pr1_mii_mt0_clk	ehrpwm2A		pr1_pru1_pru_r30[0]	pr1_pru1_pru_r31[0]	gpio2[6]	
X2	92	lcd_data1	lcd_data1	gpmc_a1	pr1_mii0_txen	ehrpwm2B		pr1_pru1_pru_r30[1]	pr1_pru1_pru_r31[1]	gpio2[7]	
X2	93	lcd_pclk	lcd_pclk	gpmc_a10	pr1_mii0_crs	pr1_edio_data_in4	pr1_edio_data_out4	pr1_pru1_pru_r30[10]	pr1_pru1_pru_r31[10]	gpio2[24]	
X2	94	lcd_vsync	lcd_vsync	gpmc_a8	gpmc_a1	pr1_edio_data_in2	pr1_edio_data_out2	pr1_pru1_pru_r30[8]	pr1_pru1_pru_r31[8]	gpio2[22]	
X2	95	lcd_ac_bias_en	lcd_ac_bias_en	gpmc_a11	pr1_mii1_crs	pr1_edio_data_in5	pr1_edio_data_out5	pr1_pru1_pru_r30[11]	pr1_pru1_pru_r31[11]	gpio2[25]	
X2	96	lcd_hsync	lcd_hsync	gpmc_a9	gpmc_a2	pr1_edio_data_in3	pr1_edio_data_out3	pr1_pru1_pru_r30[9]	pr1_pru1_pru_r31[9]	gpio2[23]	
X2	97	GND									
X2	98	GND									
X2	99	GND									
X2	100	GND									

4.2.1 Yellow and Pink Marked X1- and X2-Connectors

GPMC Pins available on X1 and X2 are shared with onboard NAND Flash and eMMC/SPI Nor.
The yellow marked Pins on X1 cannot be used freely, when NAND Flash is populated and used.
The pink marked Pins on X2 cannot be used freely, when eMMC/SPI Nor is populated and used.

For collision avoidance it is highly recommended to use the TI Pinmux tool to check your connectivity. A prepared pinmux file for byteENGINE M2 can be downloaded below.

LINK:
Prepared Pinmux File

4.3 Power Supply

- The byteENGINE can be powered with 2.5V to 5.5V.
- The recommended power supply is 5V.
- An on-board Buck/Boost converter is transforming the input voltage to 3.6V for optimal PMIC powering.
- For cost reduction, the converter and the module supplied with 3.6V can be omitted.

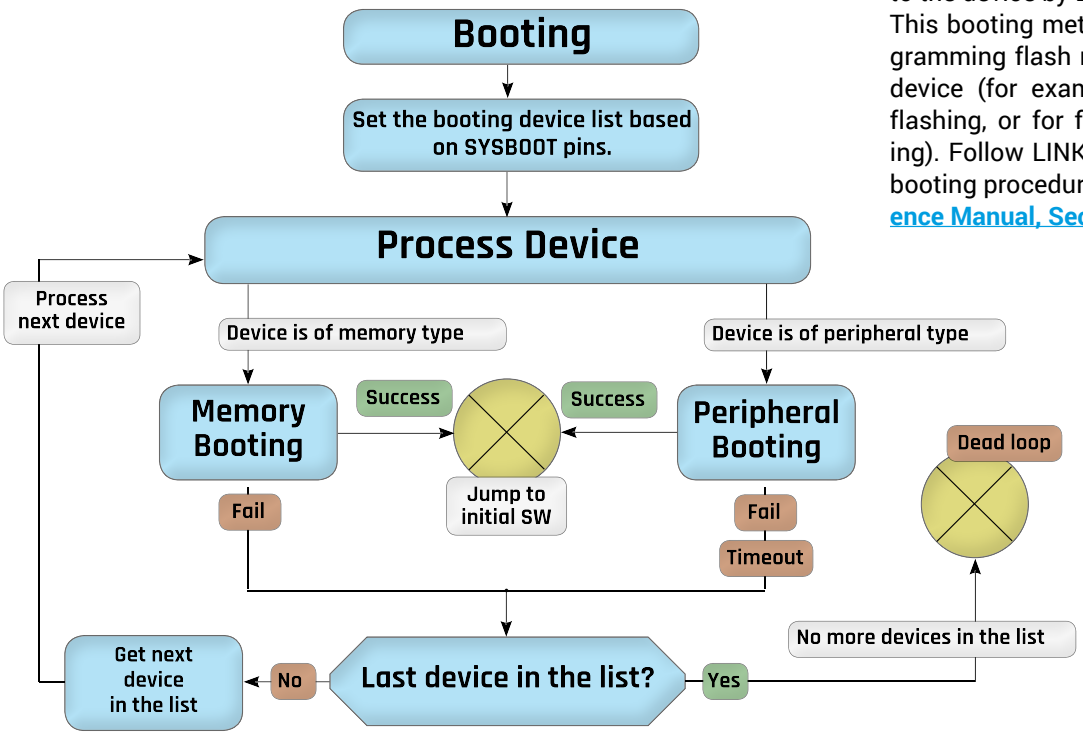
LINK:
TPS65910x Integrated Power-Management Unit

4.4 Boot Modes byteENGINE AM335x

4.4.1 Booting procedure

First a booting device list is created. The list consists of all devices which will be searched for a booting image. The list is filled in based on the SYSBOOT. Once the booting device list is set up, the booting routine examines the devices enumerated in the list sequentially and either executes the **memory booting** or **peripheral booting** procedure depending on the booting device type.

The following illustration shows the booting procedure:



- The **memory booting** procedure is executed when the booting device is a memory type like NOR, NAND, eMMC or SPI-EEPROM. If a valid booting image is found and successfully read from the external memory device, the code begins to execute.
- The **peripheral booting** is executed when the booting device type is Ethernet, USB or UART. The Data is downloaded from a host to the device by Ethernet, USB or UART links. This booting method is mostly used for programming flash memories connected to the device (for example, in the case of initial flashing, or for firmware updates or servicing). Follow LINK for details concerning this booting procedure: AM335x Technical Reference Manual, Section 26.1.9 (Page 5065)

LINK:
AM335x Technical Reference Manual

4.4.2 byteENGINE AM335x boot modes

The ROM Code creates the device list based on information gathered from the SYSBOOT configuration pins sensed in the control module. The pins are used to index the device table from which the list of devices is extracted. Table 26-7 (**Follow LINK: „Chapter 26.1.6.2.1 SYSBOOT Configuration Pins, Page 5027“.**) contains the SYSBOOT configuration pins, which correspond to LCD_DATA[0:15].

NOTICE
Be careful, when integrating the SYSBOOT configuration pins to your system. Pulling those pins high or low with your circuit can result in changed boot mode. A changed boot mode will select the wrong Boot Media. This leads to a boot failure.

Experience showed that some LCDs, also operated in reset state, can drive those pins to an undefined level. This leads to a boot failure.

To avoid the change of the boot mode, bytes at work AG highly recommends the use of a buffer with an enable pin for the SYSBOOT configuration pins.

LINK:
AM335x Technical Reference Manual

4.4.3 byteENGINE AM335x Default Boot Modes

The default boot mode setting of the byteENGINE AM335x is:

> 10011b for „Hardware revision 2.0“ (NAND, NANDI2C, MMC0, UART0)

> 10111b for „Hardware revision 4.0“ (MMC0, SPI0, UART0, USB0)

The strapping pins on the module are pulled in the default mode with 100kΩ. Furthermore, a user defined mode can be selected from Table 26-7 in the **Technical Reference Manual of the AM335x (Follow LINK: „Chapter 26.1.6.2.1 SYSBOOT Configuration Pins, Page 5027“).** When choosing a user defined boot mode, bytes at work AG advices a stronger pull resistor for the user board: (for example: 10kΩ)

LINK:
AM335x Technical Reference Manual

NOTICE
When choosing a user defined boot mode, bytes at work AG advices a stronger pull resistor for the user board.

5. Ordering Info

The Ordering Code allows the customer to recognize easily the detailed specification of the ordered SOM. Please refer to chapter **„3.4 Overview of AM335x Processors“ auf Seite 7** for possible CPU type and clock speed combinations.

[SOM]-AM335[x]_[SPEED]_R[xxx MB]_[E GB][N MB]_[C, I]

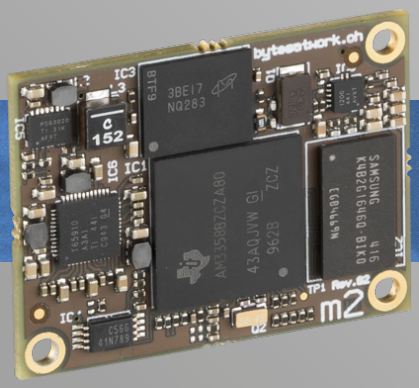
[SOM]:	SOM type	bE: byteENGINE
AM335[x]:	CPU type	2: AM3352, 4: AM3354, 6: AM3356, 8: AM3358, 9: AM3359
[SPEED MHz]:	Clock speed	300, 600, 800, 1000
R[xxx MB]:	RAM size	128, 256, 512 MB
[E GB]:	eMMC FLASH size	[E 4, 8 GB]
[N MB]:	NAND FLASH size	[N 256 MB]
[C, I]:	Temperature range	[C] Customer 0° to +70° Celsius, [I] Industrial -40° to +85° Celsius

6. References

LINKS:

>	Prepared Pinmux file for byteENGINE M2	Chapter: 3.10, 4.2.1
>	Texas Instruments Pinmux tool: https://dev.ti.com/pinmux/app.html	Chapter: 3.10
>	Detailed pinout for byteENGINE M2	Chapter: 4.1, 4.2
>	Datasheet Connectors Neltron 2001S-100G-270-020	Chapter: 3.8
>	Schematic of the connectors X1 and X2	Chapter: 3.7
>	meta-bytesatwork on github	Chapter: 3.1
>	Texas Instruments Sitara™ AM335x Processors	Chapter: 3.4
>	AM335x Technical Reference Manual	Chapter: 4.4.1, 4.4.2, 4.4.3
>	TPS65910x Integrated Power-Management Unit	Chapter: 4.3

7. Contact information



- bytes at work AG
  Technoparkstrasse 7
  CH-8406 Winterthur
  Switzerland
- Phone: +41 52 213 79 79
  Fax: +41 52 203 27 13
- eMail: info@bytesatwork.ch
- Product Information:
  www.bytesatwork.io
- Help:
  www.bytesatwork.io/support

bytesatwork