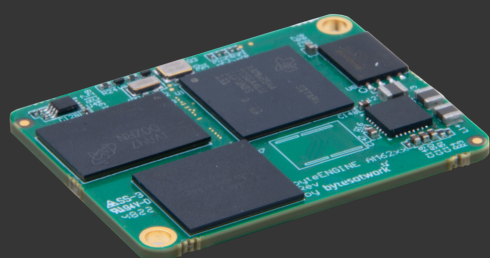


bytes**at**work

DataSheet

Rev. 2.0 06.03.2025



industrial computing module

byteENGINE AM62x

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Symbols and Typographic Conventions

These symbols represent important details or aspects for working with bytesatwork-products.



NOTICE

Follow instructions. Acting against the procedure described can lead to malfunction.



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1. Revision History

Hardware Revision	Marking on PCB	Release Date	Info
1.1	byteENGINE AM62x Rev.1.1	2023	First version available for sales
1.0	byteENGINE AM62x Rev.1.0	2022	Prototypes



NOTICE

This document refers to
byteENGINE AM62x Rev.1.1

2. Overview

2.1. General Information

The AM62x is an extension of the Sitara™ Industrial/Auto-grade family of heterogeneous Arm® processors with embedded 3D graphics acceleration, dual display interfaces and extensive peripheral and networking options. AM62x is built for a broad set of industrial and automotive applications.

AM62x contains up to four Arm® Cortex®-A53 with 64-bit, Single-core Arm® Cortex®-R5F Device Manager subsystem, IMG AXE1-16 3D graphics module, dual core PRU module and a Cortex®-M4F MCU module.

The Cortex-A53 provides powerful computing elements for Linux applications. Linux and Real-time (RT) Linux, which stays updated to the latest Long Term Support (LTS) Linux kernel, bootloader and Yocto file system.

AM62x has a powerful IMG AXE1-16 3D Graphics core for HMI applications and QT acceleration with dual display output options at resolutions up to 2K @ 60 fps.

The 2-port Gigabit Ethernet switch has one internal port and two external ports with TSN support. An additional PRU module enables real-time I/O capability. In addition, an extensive peripherals set is included in AM62x to enable system level connectivity such as USB, MMC/SD, Camera interface, OSPI, CAN-FD and GPMC for parallel host interface to an external ASIC/FPGA.

AM62x also supports secure boot for IP protection with the built-in HSM (Hardware Security Module) and also employs advanced power management support for portable and power-sensitive applications.

2.2. Technical Data

Feature

Details

CPU	Architecture	Up to Quad core 64-bit Arm® Cortex®-A53 processors
	CPU	See Link for further information: Block diagram of AM62x See TI Homepage for further Information: AM62x
	Cache	32KB L1 instruction Cache for each Core 32KB L1 Data Cache for each Core 512 kB shared L2 Cache
	Frequency (max.)	Up to 1.4 GHz
	Co-Processors	1x Cortex®-M4F MCU 400 MHz single core processor 1x Dual-Core programmable RTU with up to 333 MHz
	Security	Hardware security module: > Secure boot supported > Cryptographic acceleration supported > Trusted Execution Environment (TEE) supported > Secure storage support
GPU		IMG AXE1-16
Memory on Chip	RAM	Up to 816 KB OCSRAM
Memory External	DRAM	Up to 2 GB LPDDR4
	Flash	Up to 128 GB eMMC
	EEPROM	32 kB EEPROM
	GPMC	8 to 16 bit and up to 133 MHz
Ethernet	Speed	2x 10/100/1000 Mbps IEEE 1588
Multimedia	Display Subsystem	> Dual display support > 1920x1080 @ 60fps for each display > OLDI/LVDS (4 lanes - 2x) > 24-bit RGB parallel interface
	2D/3D Graphic Processing Unit	> Fillrate greater than 500 Mpixels/sec > 500 MTexels/s, >8 GFLOPs > Supports at least 2 composition layers > Supports up to 2048x1080 @60fps > Supports ARGB32, RGB565 and YUV formats > 2D graphics capable > OpenGL 3.x/2.0/1.1 + Extensions, Vulkan 1.2
	One Camera Serial interface (CSI-Rx) - 4 Lane with DPHY	> MIPI CSI 1.3 Compliant + MIPI-DPHY 1.2 > Support for 1,2,3 or 4 data lane mode up to 2.5Gbps > ECC verification/correction with CRC check + ECC on RAM

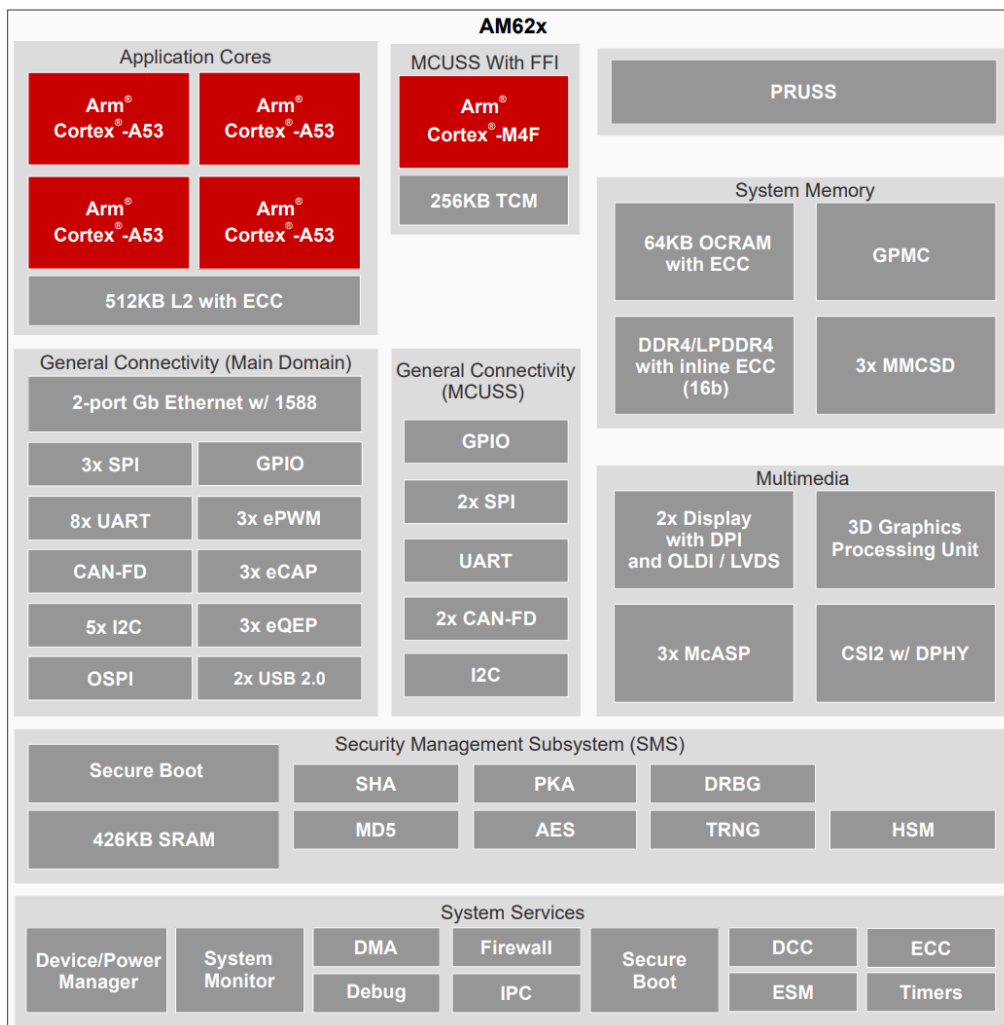
		> Virtual Channel support (up to 16) > Ability to write stream data directly to DDR via DMA
	Audio	> Transmit and Receive Clocks up to 50 MHz > Up to 16/10/6 Serial Data Pins across 3x > McASP with Independent TX and RX Clocks > Supports Time Division Multiplexing (TDM), > Inter-IC Sound (I2S), and Similar Formats > Supports Digital Audio Interface Transmission (SPDIF, IEC60958-1, and AES-3 Formats) > FIFO Buffers for Transmit and Receive (256 Bytes) > Support for audio reference output clock
Expansion	SD/SDIO, MMC, SDXC	2 x SD/SDIO (4-bits)
Functional Safety		> Developed for functional safety applications > Documentation will be available to aid IEC > 61508 functional safety system design > Systematic capability up to SIL 3 > Hardware Integrity up to SIL 2 > Safety-related certification > IEC 61508 certification by TUV SÜD planned
USB		2x USB 2.0
Serial	SPI	5
	I2C	6
	UART	9
	QSPI	1 (2x CS)
	QEP	3
	CAN-FD	3
Miscellaneous	Watchdog	Yes
	JTAG	Yes
	GPIO	Up to 198
	PWM	3
	Timer	12
	Boot Mode	Secure boot supported
Mechanical information	Input Voltage	5.0 V
	Power Consumption	4 W
	Dimensions	30 x 40 x 4 mm
	Operating Temperature	> Industrial temperature range: -40 to +85° C > Consumer temperature range: 0 to +85° C
Operating System	Linux	meta-bytesatwork available on github

2.3. Block diagram of AM62x

The AM62x from Texas Instruments is the industry's first multiprotocol gigabit (Gb) time-sensitive networking (TSN)-enabled processor family. The new, highly integrated Sitara AM62x processor provides industrial-grade reliability, with dual and quad Arm® Cortex®-A53 core variants built to meet the rapidly evolving needs of Industry 4.0 in factory automation, motor drives and grid infrastructure. The inclusion of an on-chip isolated dual-core microcontroller (MCU) subsystem enables designers to use the AM62x to create more dependable and functional safety-certifiable products while reducing overall system-level complexity.

Key features of AM62x

- > Quad Arm® Cortex®-A53 core, up to 1.4 GHz
- > Cortex®-M4 400 MHz processor
- > Imagination Technology IMG AXE1-16
- > Dual Display supported
- > Secure boot supported
- > Prepared for functional safety applications





For further information regarding the AM62x CPU, please visit the homepage of Texas Instruments:
[AM62x Sitara™ Processors datasheet \(Rev. B\)](#)

2.4. Decision guidance byteENGINE AM62x

The following five steps help identifying the suitable byteENGINE for the specific customer application.

> **Step 1:** Select the needed CPU

> **Choose Quad/Dual or Single Arm® Cortex®-A53**

Quad Core: AM62x**4**

Dual Core: AM62x**2**

Single Core: AM62x**1**

> **Choose with or without 3D-Graphics Engine**

With 3D-Graphics Engine: AM62**5**x

Without 3D-Graphics Engine: AM62**3**x

> **Step 2:** Select the needed CPU speed

> **Choose 1.0 GHz / 1.4 GHz**

> **Step 3:** Select the needed flash memory capacity

> **Choose eMMC 8 / 16 / 32 / 64 / 128 GB**

> **Step 4:** Select the needed RAM capacity

> **Choose 512 / 1024 / 1536 / 2048 MB**

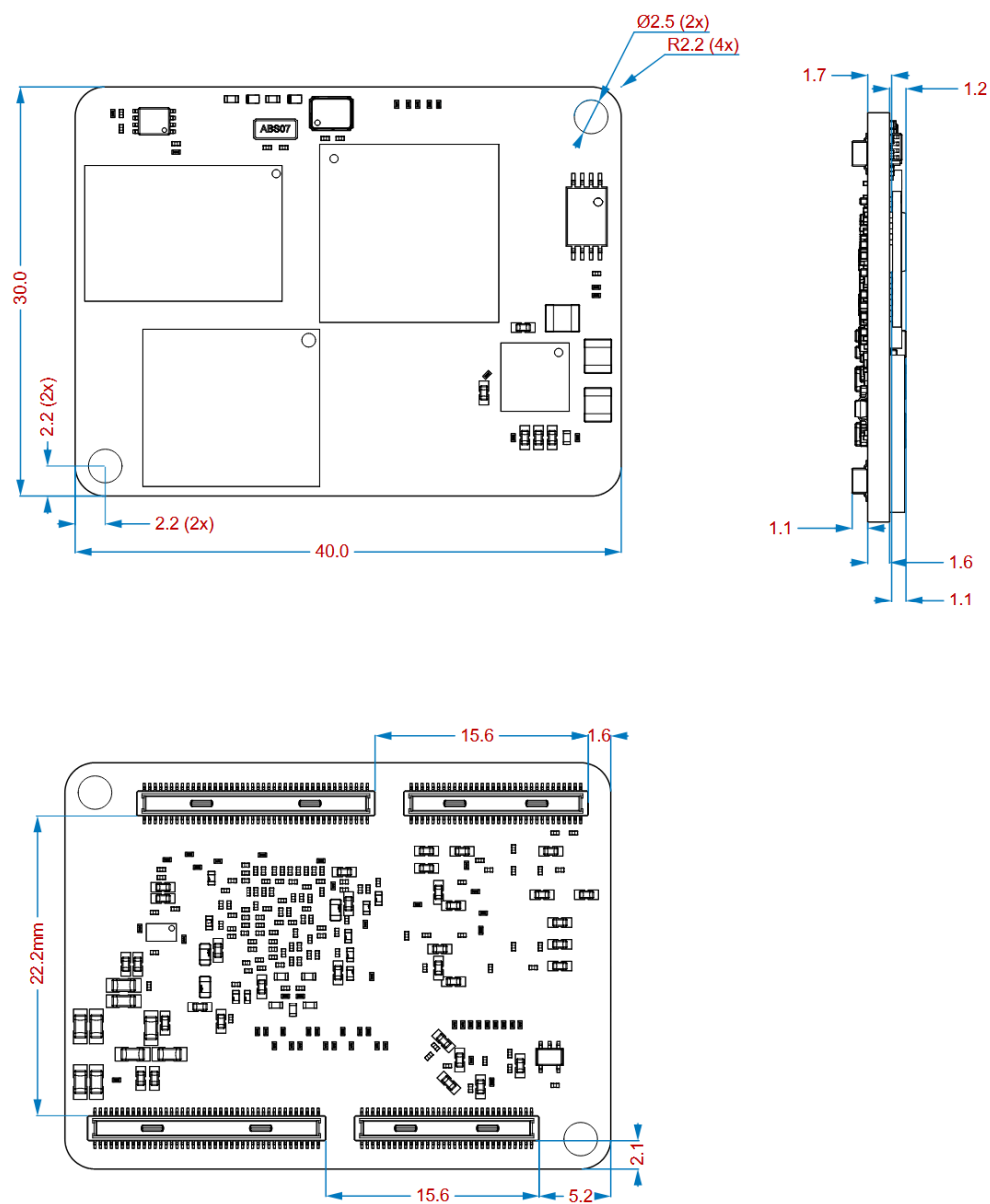
> **Step 5:** Select the needed temperature range

> **Choose consumer or industrial**

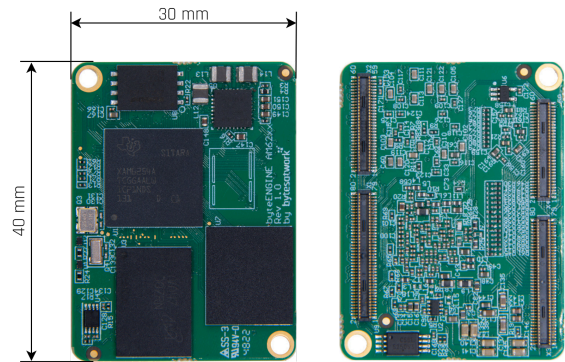
2.5. Dimensions of byteENGINE AM62x

The following illustration shows all important dimensions for mounting and installation of the industrial computing module byteENGINE AM62x.

> All dimensions are indicated in millimetres (mm)

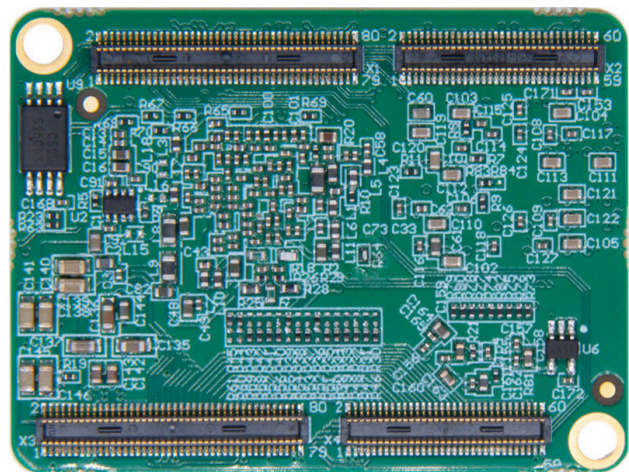


> Module design in scale 1:1:



2.6. byteENGINE AM62x connectors layout

The AM62x is connected to the carrier board with 2x 80 and 2x 60 pins on four module connectors. The following picture shows the location of the connectors on the bottom side.



Connectors

X1	Power, LVDS1, LVDS0, OSPI, CSI1, RGMII2
X2	UART0, USB1, MCU_MCAN0, MCU_MCAN1, MCAN0, JTAG, USB0, WKUP
X3	MMC1, MCU_UART0, MMC2, MDIO, RGMII1, SPI0, MCASP0
X4	LCD, GPMC, I2C1, MCU_I2C0



[Schematic of the connectors X1, X2, X3 and X4](#)

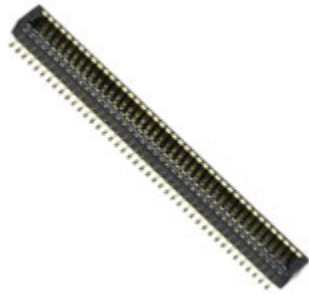


NOTICE

The module is held in the connectors with a considerable retention force. To avoid damaging the modules' connectors as well as the carrier board connectors while removing the module the use of an extraction tool is strongly recommended.

2.7. Connectors - DF40C-80DP and DF40C-60DP

The byteENGINE uses four Hirose 0,4mm Board to Board Plug connectors. For more specific information about the connectors used, please consult the datasheet of the manufacturer.



Connectors

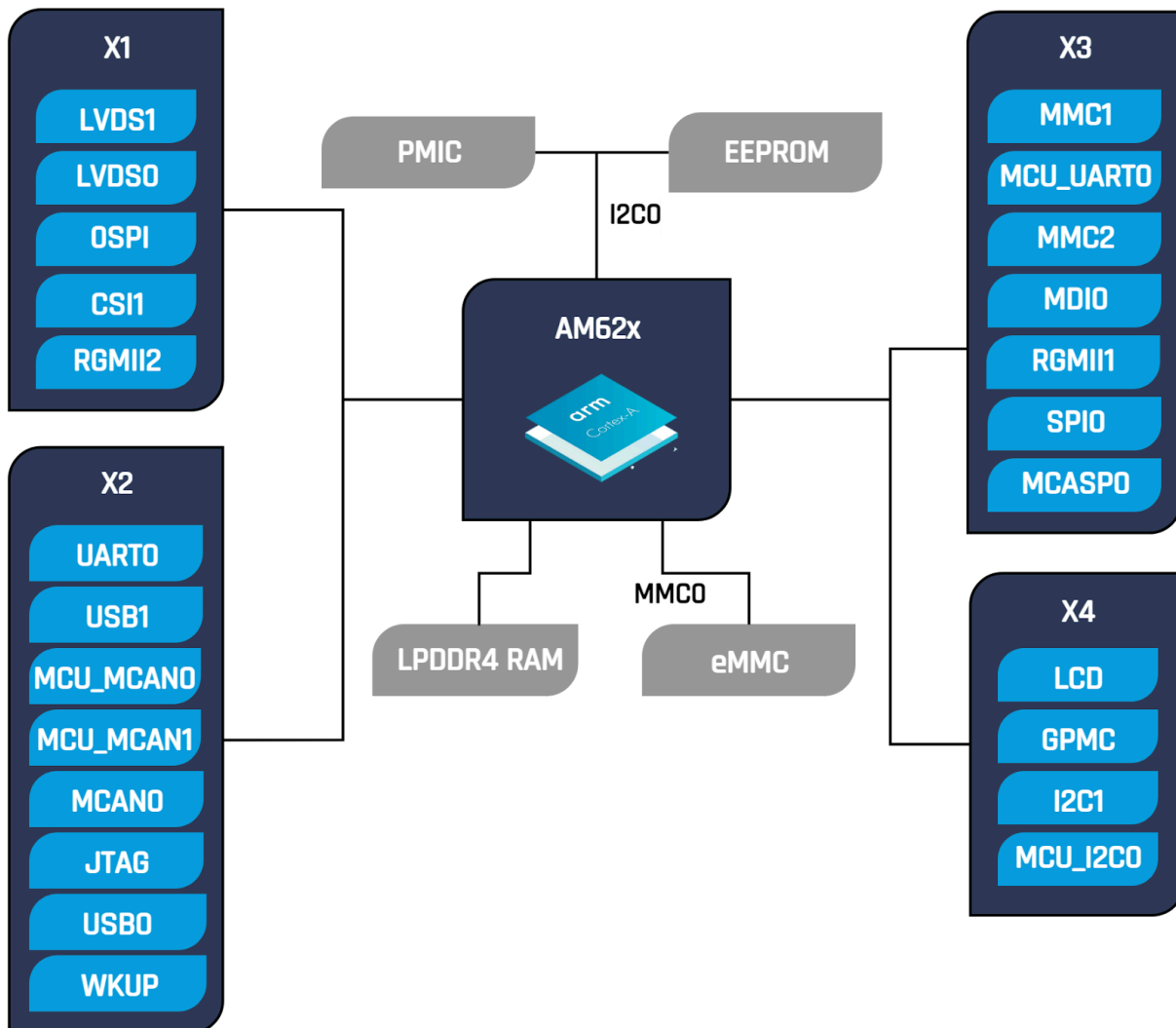
X1, X3	DF40HC(3.0)-80DS-0.4V(51)
X2, X4	DF40HC(3.0)-60DS-0.4V(51)



[Hirose DF40-Series Connectors](#)

2.8. byteENGINE AM62x Connectors Overview

The following illustration shows the „default configuration“ of the byteENGINE AM62x. The function of the components shown in gray squares cannot be changed. The blue squares show the module connectors X1, X2, X3 and X4. The functions of X1, X2, X3 and X4 can be adapted and each connector module serves multiple functions. The detailed pinout functions are shown in chapter [3. Pinout functions](#).



3. Pinout functions

3.1. Restrictions

These peripherals are internally connected and should not be utilized in the customer design if the components are populated and in use.



WARNING:

EEPROM: Production data storage. Do not use for application, readonly usage.

Restricted peripherals

I2C0 PMIC and EEPROM

MMC0 eMMC

Ball	Pin Name	Used for
B16	I2C0_SCL	PMIC/EEPROM
A16	I2C0_SDA	PMIC/EEPROM
AB1	MMC0_CLK	eMMC
Y3	MMC0_CMD	eMMC
AA2	MMC0_DAT0	eMMC
AA1	MMC0_DAT1	eMMC
AA3	MMC0_DAT2	eMMC
Y4	MMC0_DAT3	eMMC
AB2	MMC0_DAT4	eMMC
AC1	MMC0_DAT5	eMMC
AD2	MMC0_DAT6	eMMC
AC2	MMC0_DAT7	eMMC
E24	OSPI0_CSn3	VSEL_SD

3.2. Carrier board connectors X1

Con	Pin	Signal Name	Mode 0	Alternative Modes on Pin								
				1	2	3	4	5	6	7	8	9
X1	1	GND										
X1	2	GND										
X1	3	PowerButton										
X1	4	OLDI0_A7P	OLDI0_A7P									
X1	5											
X1	6	OLDI0_A7N	OLDI0_A7N									
X1	7											
X1	8	OLDI0_A6P	OLDI0_A6P									
X1	9											
X1	10	OLDI0_A6N	OLDI0_A6N									
X1	11											
X1	12	OLDI0_CLK1P	OLDI0_CLK1P									
X1	13	GND										
X1	14	OLDI0_CLK1N	OLDI0_CLK1N									
X1	15	OLDI0_A3P	OLDI0_A3P									
X1	16	OLDI0_A4P	OLDI0_A4P									
X1	17	OLDI0_A3N	OLDI0_A3N									
X1	18	OLDI0_A4N	OLDI0_A4N									
X1	19	OLDI0_A2P	OLDI0_A2P									
X1	20	OLDI0_A5P	OLDI0_A5P									
X1	21	OLDI0_A2N	OLDI0_A2N									
X1	22	OLDI0_A5N	OLDI0_A5N									
X1	23	OLDI0_CLK0P	OLDI0_CLK0P									
X1	24	GND										
X1	25	OLDI0_CLK0N	OLDI0_CLK0N									

Con	Pin	Signal Name	Mode 0	Alternative Modes on Pin								
				1	2	3	4	5	6	7	8	9
X1	26	OSPI0_CLK	OSPI0_CLK							GPIO0_0		
X1	27	OLDIO_A1P	OLDIO_A1P									
X1	28	OSPI0_D0	OSPI0_D0							GPIO0_3		
X1	29	OLDIO_A1N	OLDIO_A1N									
X1	30	OSPI0_D1	OSPI0_D1							GPIO0_4		
X1	31	OLDIO_A0P	OLDIO_A0P									
X1	32	OSPI0_D2	OSPI0_D2							GPIO0_5		
X1	33	OLDIO_A0N	OLDIO_A0N									
X1	34	OSPI0_D3	OSPI0_D3							GPIO0_6		
X1	35	GND										
X1	36	OSPI0_D4	OSPI0_D4	SPI1_CS0	MCASP1_AXR1	UART6_RXD				GPIO0_7		
X1	37											
X1	38	OSPI0_D5	OSPI0_D5	SPI1_CLK	MCASP1_AXR0	UART6_TXD				GPIO0_8		
X1	39											
X1	40	OSPI0_D6	OSPI0_D6	SPI1_D0	MCASP1_ACLKX	UART6_RTSn				GPIO0_9		
X1	41											
X1	42	OSPI0_D7	OSPI0_D7	SPI1_D1	MCASP1_AFSX	UART6_CTSn				GPIO0_10		
X1	43											
X1	44	OSPI0_CSn1	OSPI0_CSn1							GPIO0_12		
X1	45											
X1	46	OSPI0_CSn2	OSPI0_CSn2	SPI1_CS1	OSPI0_RESET_OUT1	MCASP1_AFSR	MCASP1_AXR2	UART5_RXD		GPIO0_13		
X1	47											
X1	48	OSPI0_DQS	OSPI0_DQS					UART5_CTSn		GPIO0_2		
X1	49											
X1	50	GND										
X1	51											
X1	52	OSPI0_LBCLK0	OSPI0_LBCLK0					UART5_RTSn		GPIO0_1		
X1	53											
X1	54	EXT_REFCLK1	EXT_REFCLK1	SYNC1_OUT	SPI2_CS3	SYSCLKOUT0	TIMER_I04	CLKOUT0	CP_GEMAC_CPTS0_RFT_CLK	GPIO1_30	ECAP0_IN_APWM_OUT	
X1	55	WKUP_CL-KOUT0	WKUP_CLKOUT0									

Con	Pin	Signal Name	Mode 0	Alternative Modes on Pin								
				1	2	3	4	5	6	7	8	9
X1	56	GND										
X1	57	GND										
X1	58	RGMII2_TX_CTL	RGMII2_TX_CTL	RMII2_TX_EN	MCASP2_AXR4	PR0_PRU1_GPO0	PR0_PRU1_GPI0			GPIO0_87		
X1	59	CSI0_RXP3	CSI0_RXP3									
X1	60	RGMII2_TXC	RGMII2_TXC	RMII2_CRS_DV	MCASP2_AXR5	PR0_PRU1_GPO1	PR0_PRU1_GPI1			GPIO0_88		
X1	61	CSI0_RXN3	CSI0_RXN3									
X1	62	RGMII2_TD0	RGMII2_TD0	RMII2_TXD0	MCASP2_AXR6	PR0_PRU1_GPO2	PR0_PRU1_GPI2					
X1	63	CSI0_RXP2	CSI0_RXP2									
X1	64	RGMII2_TD1	GMII2_TD1	RMII2_TXD1	MCASP2_ACLKR	PR0_PRU1_GPO3	PR0_PRU1_GPI3	MCASP2_AXR8		GPIO0_90		
X1	65	CSI0_RXN2	CSI0_RXN2									
X1	66	RGMII2_TD2	RGMII2_TD2		MCASP2_AFSX	PR0_PRU1_GPO4	PR0_PRU1_GPI4	PR0_ECAP0_IN_ APWM_OUT		GPIO0_91	EQEP2_I	
X1	67	CSI0_RXCLKP	CSI0_RXCLKP									
X1	68	RGMII2_TD3	RGMII2_TD3		MCASP2_ACLKX	PR0_PRU1_GPO16	PR0_PRU1_GPI16	PR0_ECAP0_SY NC_OUT	PR0_UART0_CTS n	GPIO1_0	EQEP2_S	
X1	69	CSI0_RXCLKN	CSI0_RXCLKN									
X1	70	RGMII2_RX_CTL	MII2_RX_CTL	RMII2_RX_ER	MCASP2_AXR3	PR0_PRU0_GPO0	PR0_PRU0_GPI0			GPIO1_1		
X1	71	CSI0_RXP1	CSI0_RXP1									
X1	72	RGMII2_RXC	RGMII2_RXC	RMII2_REF_CLK	MCASP2_AXR1	PR0_PRU0_GPO1	PR0_PRU0_GPI1	PR0_ECAP0_SYNC_I		GPIO1_2		
X1	73	CSI0_RXN1	CSI0_RXN1									
X1	74	RGMII2_RD0	RGMII2_RD0	RMII2_RXD0	MCASP2_AXR2	PR0_PRU0_GPO2	PR0_PRU0_GPI2		PR0_UART0_RTSn	GPIO1_3		
X1	75	CSI0_RXP0	CSI0_RXP0									
X1	76	RGMII2_RD1	RGMII2_RD1	RMII2_RXD1	MCASP2_AFSR	PR0_PRU0_GPO3	PR0_PRU0_GPI3	MCASP2_AXR7		GPIO1_4		
X1	77	CSI0_RXN0	CSI0_RXN0									
X1	78	RGMII2_RD2	RGMII2_RD2		MCASP2_AXR0	PR0_PRU0_GPO4	PR0_PRU0_GPI4	PR0_UART0_RXD		GPIO1_5	EQEP2_A	
X1	79	GND										
X1	80	RGMII2_RD3	RGMII2_RD3		AUDIO_EXT_REFC LK0	PR0_PRU0_GPO16	PR0_PRU0_GPI16	PR0_UART0_TXD		GPIO1_6	EQEP2_B	

3.3. Carrier board connectors X2

Con	Pin	Signal_Name	Mode 0	Alternative Modes on Pin								
				1	2	3	4	5	6	7	8	9
X2	1	GND										
X2	2	GND										
X2	3	UART0_RXD	UART0_RXD	ECAP1_IN_APWM_OUT	SPI2_D0	EHRPWM2_A				GPIO1_20		
X2	4	USB1_VBUS	USB1_VBUS									
X2	5	UART0_TXD	UART0_TXD	ECAP2_IN_APWM_OUT	SPI2_D1	EHRPWM2_B				GPIO1_21		
X2	6											
X2	7	UART0_CTSn	UART0_CTSn	SPI0_CS2	I2C3_SCL	UART2_RXD	TIMER_I06	AUDIO_EXT_REFCLK0	PR0_ECAP0_SYNC_OUT	GPIO1_22	MCASP2_AFSX	MMC2_SDCD
X2	8	USB1_DRVVBUS	USB1_DRVVBUS							GPIO1_51		
X2	9	UART0_RTSn	UART0_RTSn	SPI0_CS3	I2C3_SDA	UART2_TXD	TIMER_I07	AUDIO_EXT_REFCLK1	PR0_ECAP0_IN_APWM_OUT	GPIO1_23	MCASP2_ACLKX	MMC2_SDWP
X2	10											
X2	11	GND										
X2	12	GND										
X2	13	MCU_MCAN0_RX	MCU_MCAN0_RX	MCU_TIMER_I00	MCU_SPI1_CS3					MCU_GPIO0_14		
X2	14	USB1_DM	USB1_DM									
X2	15	MCU_MCAN0_TX	MCU_MCAN0_TX	WKUP_TIMER_I00	MCU_SPI0_CS3					MCU_GPIO0_13		
X2	16	USB1_DP	USB1_DP									
X2	17	MCU_MCAN1_RX	MCU_MCAN1_RX	MCU_TIMER_I03	MCU_SPI0_CS2	MCU_SPI1_CS2	MCU_SPI1_CLK			MCU_GPIO0_16		
X2	18	GND										
X2	19	MCU_MCAN1_TX	MCU_MCAN1_TX	MCU_TIMER_I02		MCU_SPI1_CS1	MCU_EXT_REFCLK0			MCU_GPIO0_15		
X2	20											
X2	21	GND										

Con	Pin	Signal_Name	Mode 0	Alternative Modes on Pin								
				1	2	3	4	5	6	7	8	9
X2	22											
X2	23											
X2	24	GND										
X2	25	MCAN0_RX	MCAN0_RX	UART5_TXD	TIMER_IO3	SYNC3_OUT	UART1_RIn	EQEP2_S	PR0_UART0_TXD	GPIO1_25	MCASP2_AXR1	EHRPWM_TZn_IN4
X2	26											
X2	27	MCAN0_TX	MCAN0_TX	UART5_RXD	TIMER_IO2	SYNC2_OUT	UART1_DTRn	EQEP2_I	PR0_UART0_RXD	GPIO1_24	MCASP2_AXR0	EHRPWM_TZn_IN3
X2	28											
X2	29	GND										
X2	30	GND										
X2	31	TCK	TCK									
X2	32	USB0_VBUS	USB0_VBUS									
X2	33	TMS	TMS									
X2	34											
X2	35	TDI	TDI									
X2	36	USB0_DRVVBUS	USB0_DRVVBUS							GPIO1_50		
X2	37	TDO	TDO									
X2	38											
X2	39											
X2	40	GND										
X2	41	GND										
X2	42	USB0_DM	USB0_DM									
X2	43	TRSTn	TRSTn									
X2	44	USB0_DP	USB0_DP									
X2	45	EMU0	EMU0									
X2	46	GND										
X2	47	EMU1	EMU1									
X2	48	WKUP_I2C0_SCL	WKUP_I2C0_SCL							MCU_GPIO0_19		

Con	Pin	Signal_Name	Mode 0	Alternative Modes on Pin								
				1	2	3	4	5	6	7	8	9
X2	49	MCU_ERRORn	MCU_ERRORn									
X2	50	WKUP_I2C0_SDA	WKUP_I2C0_SDA							MCU_GPIO0_20		
X2	51	MCU_RESETSTATz	MCU_RESETSTATz							MCU_GPIO0_21		
X2	52	WKUP_UART0_RXD	WKUP_UART0_RXD		MCU_SPI0_CS2					MCU_GPIO0_9		
X2	53	MCU_RESETz	MCU_RESETz									
X2	54	WKUP_UART0_TXD	WKUP_UART0_TXD		MCU_SPI1_CS2					MCU_GPIO0_10		
X2	55	PORz_OUT	PORz_OUT									
X2	56	WKUP_UART0_RTSn	WKUP_UART0_RTSn	WKUP_TIMER_I01		MCU_SPI1_CLK				MCU_GPIO0_12		
X2	57	RESET_REQz	RESET_REQz									
X2	58	WKUP_UART0_CTSn	WKUP_UART0_CTSn	WKUP_TIMER_I00		MCU_SPI1_CS0				MCU_GPIO0_11		
X2	59	GND										
X2	60	GND										

3.4. Carrier board connectors X3

Con	Pin	Signal_Name	Mode 0	Alternative Modes on Pin								
				1	2	3	4	5	6	7	8	9
X3	1	VSYS										
X3	2	VSYS										
X3	3	VSYS										
X3	4	VSYS										
X3	5	VSYS										
X3	6	VSYS										
X3	7	VSYS										
X3	8	VSYS										
X3	9	VSYS										
X3	10	VSYS										
X3	11	GND										
X3	12	GND										
X3	13	GND										
X3	14	GND										
X3	15	GND										
X3	16	GND										
X3	17	MMC1_CLK	MMC1_CLK		TIMER_I04	UART3_RXD				GPIO1_46		
X3	18	MDIO0_MDC	MDIO0_MDC							GPIO0_86		
X3	19	MMC1_CMD	MMC1_CMD		TIMER_I05	UART3_TXD				GPIO1_47		
X3	20	MDIO0_MDIO	MDIO0_MDIO							GPIO0_85		
X3	21	MMC1_DAT0	MMC1_DAT0	CP_GEMAC_CPTS0_HW2TSPUSH	TIMER_I03	UART2_CTSn	ECAP2_IN_APW_M_OUT			GPIO1_45		
X3	22	RGMII1_TX_CTL	RGMII1_TX_CTL	RMII1_TX_EN						GPIO0_73		

Con	Pin	Signal_Name	Mode 0	Alternative Modes on Pin								
				1	2	3	4	5	6	7	8	9
X3	23	MMC1_DAT1	MMC1_DAT1	CP_GEMAC_CPTS0_HW1TSPUSH	TIMER_IO2	UART2_RTSn	ECAP1_IN_APW_M_OUT			GPIO1_44		
X3	24	RGMII1_TXC	RGMII1_TXC	RMII1_CRSDV						GPIO0_74		
X3	25	MMC1_DAT2	MMC1_DAT2	CP_GEMAC_CPTS0_TS_SYNC	TIMER_IO1	UART2_TXD				GPIO1_43		
X3	26	RGMII1_TD0	RGMII1_TD0	RMII1_TXD0						GPIO0_75		
X3	27	MMC1_DAT3	MMC1_DAT3	CP_GEMAC_CPTS0_TS_COMP	TIMER_IO0	UART2_RXD				GPIO1_42		
X3	28	RGMII1_TD1	RGMII1_TD1	RMII1_TXD1						GPIO0_76		
X3	29	MMC1_SDCD	MMC1_SDCD	UART6_RXD	TIMER_IO6	UART3_RTSn				GPIO1_48		
X3	30	RGMII1_TD2	RGMII1_TD2		PR0_UART0_RXD					GPIO0_77		
X3	31	MMC1_SDWP	MMC1_SDWP	UART6_TXD	TIMER_IO7	UART3_CTSn				GPIO1_49		
X3	32	RGMII1_TD3	RGMII1_TD3		PR0_UART0_TXD					GPIO0_78		
X3	33	MCU_UART0_RXD	MCU_UART0_RXD							MCU_GPIO0_5		
X3	34	RGMII1_RX_CTL	RGMII1_RX_CTL	RMII1_RX_ER						GPIO0_79		
X3	35	MCU_UART0_TXD	MCU_UART0_TXD							MCU_GPIO0_6		
X3	36	RGMII1_RXC	RGMII1_RXC	RMII1_REF_CLK	PR0_UART0_CTSn					GPIO0_80		
X3	37	MCU_UART0_CTSn	MCU_UART0_CTSn	MCU_TIMER_IO0		MCU_SPI1_D0				MCU_GPIO0_7		
X3	38	RGMII1_RD0	RGMII1_RD0	RMII1_RXD0						GPIO0_81		
X3	39	MCU_UART0_RTSn	MCU_UART0_RTSn	MCU_TIMER_IO1		MCU_SPI1_D1				MCU_GPIO0_8		
X3	40	RGMII1_RD1	RGMII1_RD1	RMII1_RXD1						GPIO0_82		
X3	41	GND										
X3	42	RGMII1_RD2	RGMII1_RD2		PR0_UART0_RTSn					GPIO0_83		
X3	43	MMC2_CLK	MMC2_CLK	MCASP1_ACLKR	MCASP1_AXR5	UART6_RXD				GPIO0_69		
X3	44	RGMII1_RD3	RGMII1_RD3							GPIO0_84		
X3	45	MMC2_CMD	MMC2_CMD	MCASP1_AFSR	MCASP1_AXR4	UART6_TXD				GPIO0_70		
X3	46	SPI0_CS1	SPI0_CS1	CP_GEMAC_CPTS0_TS_COMP	EHRPWM0_B	ECAP0_IN_APW_M_OUT				GPIO1_16		EHRPWM_T_Zn_IN5

Con	Pin	Signal_Name	Mode 0	Alternative Modes on Pin								
				1	2	3	4	5	6	7	8	9
X3	47	MMC2_DAT0	MMC2_DAT0	MCASP1_AXR0						GPIO0_68		
X3	48	SPI0_CS0	SPI0_CS0		EHRPWM0_A				PR0_ECAP0_SYNC_IN	GPIO1_15		
X3	49	MMC2_DAT1	MMC2_DAT1	MCASP1_AXR1						GPIO0_67		
X3	50	SPI0_D0	SPI0_D0	CP_GEMAC_CPTS0_HW1TSPUSH	EHRPWM1_B					GPIO1_18		
X3	51	MMC2_DAT2	MMC2_DAT2	MCASP1_AXR2		UART5_TXD				GPIO0_66		
X3	52	SPI0_D1	SPI0_D1	CP_GEMAC_CPTS0_HW2TSPUSH	EHRPWM_TZn_IN0					GPIO1_19		
X3	53	MMC2_DAT3	MMC2_DAT3	MCASP1_AXR3		UART5_RXD				GPIO0_65		
X3	54	SPI0_CLK	SPI0_CLK	CP_GEMAC_CPTS0_TS_SYNC	EHRPWM1_A					GPIO1_17		
X3	55	MMC2_SDCD	MMC2_SDCD	MCASP1_ACLKX		UART4_RXD				GPIO0_71		
X3	56	MCU_SPI0_CS1	MCU_SPI0_CS1	MCU_OBSCLK0	MCU_SYSCLKOUT0	MCU_EXT_REFCLK0	MCU_TIMER_IO1			MCU_GPIO0_1		
X3	57	MMC2_SDWP	MMC2_SDWP	MCASP1_AFSX		UART4_TXD				GPIO0_72		
X3	58	MCU_SPI0_CS0	MCU_SPI0_CS0				WKUP_TIMER_I01			MCU_GPIO0_0		
X3	59											
X3	60	MCU_SPI0_D1	MCU_SPI0_D1							MCU_GPIO0_4		
X3	61	VSELECT										
X3	62	MCU_SPI0_D0	MCU_SPI0_D0							MCU_GPIO0_3		
X3	63	VDD_3V3										
X3	64	MCU_SPI0_CLK	MCU_SPI0_CLK							MCU_GPIO0_2		
X3	65	VDD_IO										
X3	66	MCASP0_AXR2	MCASP0_AXR2	SPI2_D1	UART1_RTSn	UART6_TXD	PR0_IEP0_EDIO_DATA_IN_OUT29	ECAP2_IN_APWM_OUT	PR0_UART0_TXD	GPIO1_8	EQEP0_B	
X3	67	VMMC_IO										
X3	68	MCASP0_AXR3	MCASP0_AXR3	SPI2_D0	UART1_CTSn	UART6_RXD	PR0_IEP0_EDIO_DATA_IN_OUT28	ECAP1_IN_APWM_OUT	PR0_UART0_RXD	GPIO1_7	EQEP0_A	
X3	69	VPP										

Con	Pin	Signal_Name	Mode 0	Alternative Modes on Pin								
				1	2	3	4	5	6	7	8	9
X3	70	MCASP0_AFSX	MCASP0_AFSX	SPI2_CS3	AUDIO_EXT_REFC LK1					GPIO1_12	EQEP1_B	
X3	71	GND										
X3	72	MCASP0_ACLKX	MCASP0_ACLKX	SPI2_CS1	ECAP2_IN_AP WM_OUT					GPIO1_11	EQEP1_A	
X3	73											
X3	74	MCASP0_AXR1	MCASP0_AXR1	SPI2_CS2	ECAP1_IN_AP WM_OUT			PR0_UART0_RXD	EHRPWM1_A	GPIO1_9	EQEP0_S	
X3	75											
X3	76	MCASP0_AFSR	MCASP0_AFSR	SPI2_CS0	UART1_RXD				EHRPWM0_A	GPIO1_13	EQEP1_S	
X3	77											
X3	78	MCASP0_ACLKR	MCASP0_ACLKR	SPI2_CLK	UART1_TXD				EHRPWM0_B	GPIO1_14	EQEP1_I	
X3	79	GND										
X3	80	MCASP0_AXR0	MCASP0_AXR0	PR0_ECAP0_IN_AP WM_OUT	AUDIO_EXT_REFC LK0			PR0_UART0_TXD	EHRPWM1_B	GPIO1_10	EQEP0_I	

3.5. Carrier board connectors X4

Con	Pin	Signal_Name	Mode 0	Alternative Modes on Pin								
				1	2	3	4	5	6	7	8	9
X4	1	GND										
X4	2	GPMC0_CLK	GPMC0_CLK		MCASP1_AXR3	GPMC0_FCLK_MUX	PR0_PRU0_GPO8	PR0_PRU0_GPI8	TRC_DATA6	GPIO0_31		
X4	3	VOUT0_DATA0	VOUT0_DATA0	GPMC0_A0	PR0_PRU1_GPO0	PR0_PRU1_GPI0	UART2_RXD	PR0_PRU0_GPO8	PR0_PRU0_GPI8	GPIO0_45		
X4	4	GPMC0_AD0	GPMC0_AD0	PR0_PRU1_GPO8	PR0_PRU1_GPI8	MCASP2_AXR4	PR0_PRU0_GPO0	PR0_PRU0_GPI0	TRC_CLK	GPIO0_15		
X4	5	VOUT0_DATA1	VOUT0_DATA1	GPMC0_A1	PR0_PRU1_GPO1	PR0_PRU1_GPI1	UART2_TXD	PR0_PRU0_GPO9	PR0_PRU0_GPI9	GPIO0_46		
X4	6	GPMC0_AD1	GPMC0_AD1	PR0_PRU1_GPO9	PR0_PRU1_GPI9	MCASP2_AXR5	PR0_PRU0_GPO1	PR0_PRU0_GPI1	TRC_CTL	GPIO0_16		
X4	7	VOUT0_DATA2	VOUT0_DATA2	GPMC0_A2	PR0_PRU1_GPO2	PR0_PRU1_GPI2	UART3_RXD	PR0_PRU0_GPO10	PR0_PRU0_GPI10	GPIO0_47		
X4	8	GPMC0_AD2	GPMC0_AD2	PR0_PRU1_GPO10	PR0_PRU1_GPI10	MCASP2_AXR6	PR0_PRU0_GPO2	PR0_PRU0_GPI2	TRC_DATA0	GPIO0_17		
X4	9	VOUT0_DATA3	VOUT0_DATA3	GPMC0_A3	PR0_PRU1_GPO3	PR0_PRU1_GPI3	UART3_TXD	PR0_PRU0_GPO11	PR0_PRU0_GPI11	GPIO0_48		
X4	10	GPMC0_AD3	GPMC0_AD3	PR0_PRU1_GPO11	PR0_PRU1_GPI11	MCASP2_AXR7	PR0_PRU0_GPO3	PR0_PRU0_GPI3	TRC_DATA1	GPIO0_18		
X4	11	VOUT0_DATA4	VOUT0_DATA4	GPMC0_A4	PR0_PRU1_GPO4	PR0_PRU1_GPI4	UART4_RXD	PR0_PRU0_GPO12	PR0_PRU0_GPI12	GPIO0_49		
X4	12	GPMC0_AD4	GPMC0_AD4	PR0_PRU1_GPO12	PR0_PRU1_GPI12	MCASP2_AXR8	PR0_PRU0_GPO4	PR0_PRU0_GPI4	TRC_DATA2	GPIO0_19		
X4	13	VOUT0_DATA5	VOUT0_DATA5	GPMC0_A5	PR0_PRU1_GPO5	PR0_PRU1_GPI5	UART4_TXD	PR0_PRU0_GPO13	PR0_PRU0_GPI13	GPIO0_50		
X4	14	GPMC0_AD5	GPMC0_AD5	PR0_PRU1_GPO13	PR0_PRU1_GPI13	MCASP2_AXR9	PR0_PRU0_GPO5	PR0_PRU0_GPI5	TRC_DATA3	GPIO0_20		
X4	15	VOUT0_DATA6	VOUT0_DATA6	GPMC0_A6	PR0_PRU1_GPO6	PR0_PRU1_GPI6	UART5_RXD	PR0_PRU0_GPO14	PR0_PRU0_GPI14	GPIO0_51		
X4	16	GND										
X4	17	VOUT0_DATA7	VOUT0_DATA7	GPMC0_A7	PR0_PRU1_GPO7	PR0_PRU1_GPI7	UART5_TXD	PR0_PRU0_GPO15	PR0_PRU0_GPI15	GPIO0_52		
X4	18	GPMC0_AD6	GPMC0_AD6	PR0_PRU1_GPO14	PR0_PRU1_GPI14	MCASP2_AXR10	PR0_PRU0_GPO6	PR0_PRU0_GPI6	TRC_DATA4	GPIO0_21		
X4	19	VOUT0_DATA8	VOUT0_DATA8	GPMC0_A8	PR0_PRU1_GPO16	PR0_PRU1_GPI16	UART6_RXD	PR0_PRU0_GPO17	PR0_PRU0_GPI17	GPIO0_53		
X4	20	GPMC0_AD7	GPMC0_AD7	PR0_PRU1_GPO15	PR0_PRU1_GPI15	MCASP2_AXR11	PR0_PRU0_GPO7	PR0_PRU0_GPI7	TRC_DATA5	GPIO0_22		
X4	21	VOUT0_DATA9	VOUT0_DATA9	GPMC0_A9	PR0_PRU1_GPO8	PR0_PRU1_GPI8	UART6_TXD	PR0_PRU0_GPO16	PR0_PRU0_GPI16	GPIO0_54		
X4	22	GPMC0_AD8	GPMC0_AD8	VOUT0_DATA16	UART2_RXD	MCASP2_AXR0	PR0_PRU1_GPO0	PR0_PRU1_GPI0		GPIO0_23		
X4	23	VOUT0_DATA10	VOUT0_DATA10	GPMC0_A10	PR0_PRU1_GPO9	PR0_PRU1_GPI9	UART6_RTSn	PR0_PRU0_GPO0	PR0_PRU0_GPI0	GPIO0_55		

Con	Pin	Signal_Name	Mode 0	Alternative Modes on Pin								
				1	2	3	4	5	6	7	8	9
X4	24	GPMC0_AD9	GPMC0_AD9	VOUT0_DATA17	UART2_TXD	MCASP2_AXR1	PR0_PRU1_GPO1	PR0_PRU1_GPI1		GPIO0_24		
X4	25	VOUT0_DATA11	VOUT0_DATA11	GPMC0_A11	PR0_PRU1_GPO10	PR0_PRU1_GPI10	UART6_CTSn	PR0_PRU0_GPO1	PR0_PRU0_GPI1	GPIO0_56		
X4	26	GPMC0_AD10	GPMC0_AD10	VOUT0_DATA18	UART3_RXD	MCASP2_AXR2	PR0_PRU1_GPO2	PR0_PRU1_GPI2		GPIO0_25	OBSCLK0	
X4	27	VOUT0_DATA12	VOUT0_DATA12	GPMC0_A12	PR0_PRU1_GPO11	PR0_PRU1_GPI11	UART5_RTSn	PR0_PRU0_GPO2	PR0_PRU0_GPI2	GPIO0_57		
X4	28	GPMC0_AD11	GPMC0_AD11	VOUT0_DATA19	UART3_TXD	MCASP2_AXR3	PR0_PRU1_GPO3	PR0_PRU1_GPI3	TRC_DATA23	GPIO0_26		
X4	29	VOUT0_DATA13	VOUT0_DATA13	GPMC0_A13	PR0_PRU1_GPO12	PR0_PRU1_GPI12	UART5_CTSn	PR0_PRU0_GPO3	PR0_PRU0_GPI3	GPIO0_58		
X4	30	GPMC0_AD12	GPMC0_AD12	VOUT0_DATA20	UART4_RXD	MCASP2_AFSX	PR0_PRU0_GPO0	PR0_PRU0_GPI0	TRC_DATA22	GPIO0_27		
X4	31	VOUT0_DATA14	VOUT0_DATA14	GPMC0_A14	PR0_PRU1_GPO13	PR0_PRU1_GPI13	UART4_RTSn	PR0_PRU0_GPO4	PR0_PRU0_GPI4	GPIO0_59		
X4	32	GPMC0_AD13	GPMC0_AD13	VOUT0_DATA21	UART4_TXD	MCASP2_ACLKX	PR0_PRU0_GPO1	PR0_PRU0_GPI1	TRC_DATA21	GPIO0_28		
X4	33	VOUT0_DATA15	VOUT0_DATA15	GPMC0_A15	PR0_PRU1_GPO14	PR0_PRU1_GPI14	UART4_CTSn	PR0_PRU0_GPO5	PR0_PRU0_GPI5	GPIO0_60		
X4	34	GPMC0_AD14	GPMC0_AD14	VOUT0_DATA22	UART5_RXD	MCASP2_AFSR	PR0_PRU0_GPO2	PR0_PRU0_GPI2	TRC_DATA20	GPIO0_29	UART2_CTSn	
X4	35	VOUT0_PCLK	VOUT0_PCLK	GPMC0_A19	PR0_PRU1_GPO19	PR0_PRU1_GPI19	UART2_CTSn	PR0_PRU0_GPO19	PR0_PRU0_GPI19	GPIO0_64	PR0_ECAP0_I_N_APWM_OUT	
X4	36	GPMC0_AD15	GPMC0_AD15	VOUT0_DATA23	UART5_TXD	MCASP2_ACLKR	PR0_PRU0_GPO3	PR0_PRU0_GPI3	TRC_DATA19	GPIO0_30	UART2_RTSn	
X4	37	VOUT0_DE	VOUT0_PCLK	GPMC0_A19	PR0_PRU1_GPO19	PR0_PRU1_GPI19	UART2_CTSn	PR0_PRU0_GPO19	PR0_PRU0_GPI19	GPIO0_64	PR0_ECAP0_I_N_APWM_OUT	
X4	38	GPMC0_CSn0	GPMC0_CSn0			MCASP2_AXR14	PR0_PRU0_GPO17	PR0_PRU0_GPI17	TRC_DATA15	GPIO0_88		
X4	39	VOUT0_VSYNC	VOUT0_VSYNC	GPMC0_A18	PR0_PRU1_GPO18	PR0_PRU1_GPI18	UART2_RTSn	PR0_PRU0_GPO18	PR0_PRU0_GPI18	GPIO0_63		
X4	40	GPMC0_CSn1	GPMC0_CSn1	PR0_PRU1_GPO16	PR0_PRU1_GPI16	MCASP2_AXR15	PR0_PRU0_GPO18	PR0_PRU0_GPI18	TRC_DATA16	GPIO0_42		
X4	41	VOUT0_HSYNC	VOUT0_HSYNC	GPMC0_A16	PR0_PRU1_GPO15	PR0_PRU1_GPI15	UART3_RTSn	PR0_PRU0_GPO6	PR0_PRU0_GPI6	GPIO0_61		
X4	42	GPMC0_CSn2	GPMC0_CSn2	I2C2_SCL	MCASP1_AXR4	UART4_RXD	PR0_PRU0_GPO19	PR0_PRU0_GPI19	TRC_DATA17	GPIO0_43	MCASP1_AF	
X4	43											
X4	44	GPMC0_CSn3	GPMC0_CSn3	I2C2_SDA	GPMC0_A20	UART4_TXD	MCASP1_AXR5		TRC_DATA18	GPIO0_44	MCASP1_ACLKR	
X4	45	GND										
X4	46	GPMC0_ADVn_AL_E	GPMC0_ADVn_AL_E		MCASP1_AXR2		PR0_PRU0_GPO9	PR0_PRU0_GPI9	TRC_DATA7	GPIO0_32		
X4	47	I2C1_SCL	I2C1_SCL	UART1_RXD	TIMER_IO0	SPI2_CS1	EHRPWM0_SYNCI			GPIO1_28	EHRPWM2_A	MMC2_SDCD

Con	Pin	Signal_Name	Mode 0	Alternative Modes on Pin								
				1	2	3	4	5	6	7	8	9
X4	48	GPMC0_BE0n_CLE	GPMC0_BE0n_CLE		MCASP1_ACLKX		PR0_PRU0_GP012	PR0_PRU0_GPI12	TRC_DATA10	GPI00_35		
X4	49	I2C1_SDA	I2C1_SDA	UART1_TXD	TIMER_IO1	SPI2_CLK	EHRPWM0_SYNC_O			GPI01_29	EHRPWM2_B	MMC2_SDWP
X4	50	GPMC0_BE1n	GPMC0_BE1n			MCASP2_AXR12	PR0_PRU0_GP013	PR0_PRU0_GPI13	TRC_DATA11	GPI00_36		
X4	51	MCU_I2C0_SCL	MCU_I2C0_SCL							MCU_GPI00_17		
X4	52	GPMC0_DIR	GPMC0_DIR	PR0_ECAP0_IN_APWM_OUT		MCASP2_AXR13	PR0_PRU0_GP016	PR0_PRU0_GPI16	TRC_DATA14	GPI00_40	EQEP2_S	
X4	53	MCU_I2C0_SDA	MCU_I2C0_SDA							MCU_GPI00_18		
X4	54	GPMC0_WAIT0	GPMC0_WAIT0		MCASP1_AFSX		PR0_PRU0_GP014	PR0_PRU0_GPI14	TRC_DATA12	GPI00_37		
X4	55	GPMC0_WEn	GPMC0_WEn		MCASP1_AXR0		PR0_PRU0_GP011	PR0_PRU0_GPI11	TRC_DATA9	GPI00_34		
X4	56	GPMC0_WAIT1	GPMC0_WAIT1	VOU00_EXT_PCLKIN	GPMC0_A21	UART6_RXD				GPI00_38	EQEP2_I	
X4	57	GPMC0_OEn_REn	GPMC0_OEn_REn		MCASP1_AXR1		PR0_PRU0_GP010	PR0_PRU0_GPI10	TRC_DATA8	GPI00_33		
X4	58	GPMC0_WPn	GPMC0_WPn	AUDIO_EXT_REFCLK1	GPMC0_A22	UART6_TXD	PR0_PRU0_GP015	PR0_PRU0_GPI15	TRC_DATA13	GPI00_39		
X4	59	GND										
X4	60	GND										

3.6. Power Supply

- > The byteENGINE can be powered with 3.3V to 5.5V.
- > The recommended power supply is 5V.

3.7. Boot Modes byteENGINE AM62x

- > Bootmode Pins B15 - B0 are GPMC0_AD[0...15]

2.2x2BOOTMODE Pin Mapping

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Reserved		Backup Boot Mode Config	Backup Boot Mode			Primary Boot Mode Config			Primary Boot mode				PLL Config (b011 → 25 MHz on SOM)		



See chapter 5.3.1 of the Technical Reference Manual for more Details:
[Technical Reference Manual](#)

Primary Boot Mode	B9	B8	B7	B6	B5	B4	B3
MMCSd	1	0	0	1	0	0	0
QSPI	0	1	0	0	0	1	0
UART	0	0	0	0	1	1	1
Ethernet RMII	0	0	0	0	1	0	1
eMMC	0	0	0	1	0	0	1
USB	0	0	0	1	0	1	0

Backup BootMode	B13	B12	B11	B10
MMCSd	1	1	0	1
UART	0	0	1	1
USB DFU	0	0	0	1

B3 - B0 are set on CPU Module and should not be strapped.

4. Ordering info

The Order Code allows customers to easily recognize the detailed specification of the ordered SOM. Please refer to chapter [Decision guidance byteENGINE AM62x](#) for further information.

byteENGINE-AM62[TYPE]-[SPEED]-[RAM]-[FLASH]-[temp-range]-[revision]

[TYPE]	CPU type	AM6231 / AM6232 / AM6234 / AM6251 / AM6252 / AM6254
[SPEED]	Clock speed	1.0 GHz / 1.4 GHz
[RAM]	RAM size	512 / 768 / 1024 / 1536 / 2048 MB
[FLASH]	eMMC flash size	8 / 16 / 32 / 64 / 128 GB
[temp-range]	Temperature range	[C] Consumer 0° to +85° C [I] Industrial -40°C to +85 °C
[revision]	Revision	1.1

5. References



Notice

Files can only be downloaded with login credentials. Please request your download credentials via support@bytesatwork.ch or contact your sales representative



Links

- > Schematic of the connectors X1, X2, X3, X4:
[Schematic of the connectors](#)
- > Altium Schematic of the connectors X1, X2, X3, X4:
[Altium Schematic of the connectors](#)
- > Altium Library:
[Altium Library](#)
- > STEP Model:
[STEP Model](#)
- > Detailed Pinout of byteENGINE AM62x:
[Detailed Pinout of byteENGINE AM62x](#)
- > Texas Instruments AM62x Family:
<https://www.ti.com/product/AM625>
- > bytesatwork on github:
<https://github.com/bytesatwork>
- > byteWIKI:
<https://bytewiki.readthedocs.io/en/latest/som/am62x.html>



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Help

bytewiki.readthedocs.io