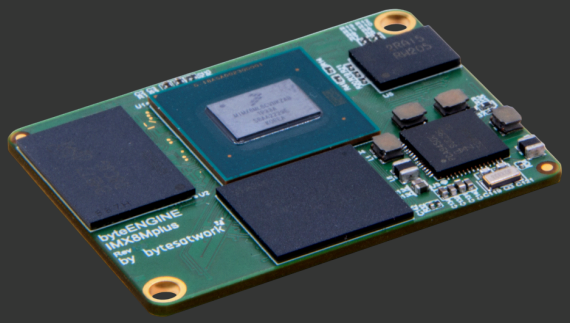
bytesatwork

Datasheet



industrial computing module

byteENGINE IMX8MP

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Symbols and Typographic Conventions

These symbols represent important details or aspects for working with bytesatwork-products.

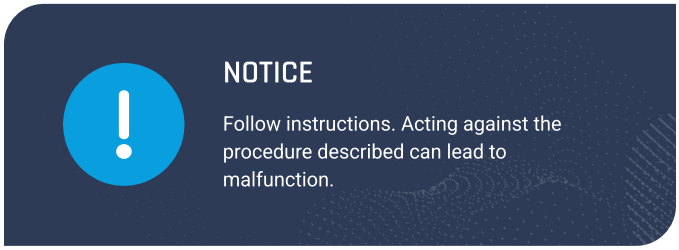

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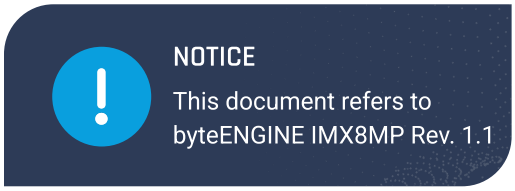
Table of Contents

1. Revision History

Hardware Revision	Marking on PCB	Release Date	Info
1.1	Rev. 1.1	February 2025	Support warm Reset from button
1.0	Rev 1.0	June 2023	First version available for sales



2. Overview

2.1. General Information

The byteENGINE IMX8MP is a high performance industrial oriented computing module. It allows you a short time-to-market, reducing development costs and substantial design risks.

The system on module uses the i.MX 8M Plus devices which are based on the high-performance dual- or quad core ARM® Cortex®-A53 64-bit RISC core operating at up to 1.8 GHz. The devices of the i.MX 8M Plus family also embed a Cortex®-M7 32-bit RISC core operating at up to 800 MHz frequency. The Cortex®-M7 core features a floating point unit (FPU) single precision which supports ARM® single-precision data-processing instructions and data types.

Furthermore, the devices of the i.MX 8M Plus family embed a 3D graphic processing unit (Vivante® - OpenGL® ES 3.0) running at up to 1 GHz, with performances up to 166 Mtriangle/s, 1 Gpixel/s.

2.2. Technical Data

Feature		Details
CPU	Architecture	Up to quad ARM® Cortex®-A53 ARM® Cortex®-M7
	CPU	i.MX 8M Plus See LINK for further information:Block diagram of i.MX 8M Plus See NXP Homepage for further information: i.MX 8M Plus
	Cache	> 32 KB L1 Instruction Cache > 32 KB L1 Data Cache > 512 kB unified L2 Cache
	Frequency (max.)	1.8 GHz
	Floating Point	Floating Point Unit (FPU) with support of the VFPv4-D16 architecture
	Co Processor	Cortex®-M7 CPU operating up to 800 MHz > 32 KB L1 Instruction Cache/ 32 KB L1 Data Cache/ 256 KB tightly coupled memory
	Security	Arm® TrustZone® (TZ) architecture, High Assurance Boot (HAB)
GPU		3D: GC7000UL with OpenCL and Vulkan support 2D: GC520
NPU		2.3 TOP/s Neural Network performance > Keyword detect, noise reduction, beamforming > Speech recognition (i.e. Deep Speech 2) > Image recognition (i.e. ResNet-50)
ISP		> 375 Mpixel/s HDR ISP supporting configurations, such as 12MP@30fps, 4kp45, or 2x 1080p80
Memory External	DRAM	32-bit LPDDR4-4000 (up to 8 GB)
	Flash	up to 128 GB eMMC
Ethernet	Speed	1 x 10/100/1000 Mbps & IEEE 1588 1 x 10/100/1000 Mbps & IEEE 1588 with TSN
Multimedia	Video Processing Unit	Video Decode > 1080p60 HEVC/H.265 Main, Main 10 (up to level 5.1) > 1080p60 VP9 Profile 0, 2 > 1080p60 VP8 • 1080p60 AVC/H.264 Baseline, Main, High decoder Video Encode > 1080p60 AVC/H.264 encoder > 1080p60 HEVC/H.265 encoder
	Graphic Processing Unit	> Supports OpenGL ES 1.1, 2.0, 3.0 and OpenCL 1.2, Vulkan

	LCDIF Display Controller	> One LCDIF drives MIPI DSI, up to UWHD and WUXGA > One LCDIF drives LVDS Tx, up to 1920x1080p60 > One LCDIF drives HDMI Tx, up to 4kp30
	Audio	> Cadence® Tensilica® HiFi 4 DSP, operating up to 800 MHz > SPDIF input and output, including a raw capture input mode > Six external synchronous audio interface (SAI) modules supporting I2S, AC97, TDM, codec/DSP, and DSD interfaces, comprising one SAI with 8 TX and 8 RX lanes, one SAI with 4 TX and 4 RX lanes, two SAI with 2 TX and 2 RX lanes, and two SAI with 1 TX and 1RX lane. > All ports support 49.152 MHz BCLK. > ASRC supports processing 32 audio channels, 4 context groups, 8 kHz to 384 kHz sample rate, and 1/16 to 8x sample rate conversion ratio. > eARC/ARC > 8-channel PDM mic input
Expansion	**SD/SDIO 3.0**	2
Serial	**SPI**	3
	I2C	6
	UART	4
	OctalSPI	1
	PCI Express (Gen3, single lane)	1
USB	**2x USB 3.0 / 2.0**	2
HDMI		HDMI 2.0a Tx supporting one display (eARC) > Resolutions of: 720 x 480p60, 1280 x 720p60, 1920 x 1080p60, 1920 x 1080p120, 3840 x 2160p30 > Pixel clock up to 297 MHz Audio support > 32-channel audio output support > 1 SPDIF audio eARC input support
Miscellaneous	**Watchdog**	3
	Secure JTAG	Yes
	GPIO (5 x 32 Bit)	160 GPIOs available (see detailed pinout and restrictions in chapter 3)
	PWM	4
	Timer	6
	Boot Mode	High Assurance Boot (HAB)
	Temperature Probe	2
Mechanical Information	**Input Voltage**	5.0 V
	Power Consumption	4 W

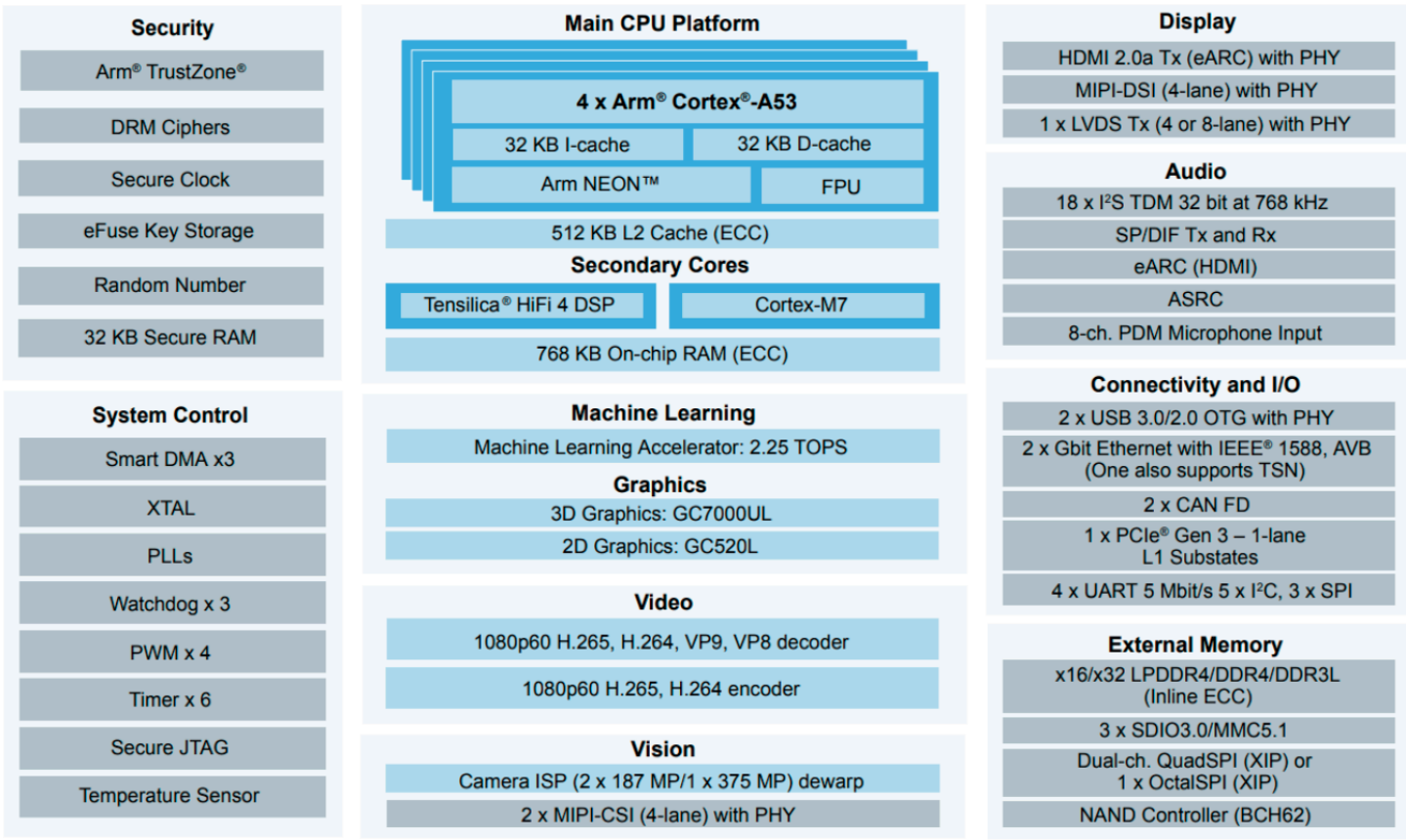
	Dimensions	30 x 40 mm
	Operating Temperature	> Industrial temperature range: -40 to +85° C > Consumer temperature range: 0 to 85° C
	Connector	2x 80 PIN, 2x 60 PIN
Operating System	**Linux**	https://github.com/bytesatwork/meta-bytesatwork

2.3. Block diagram of i.MX 8M Plus

The i.MX 8M Plus family focuses on neural processing unit (NPU) and vision systems, advanced multimedia, and industrial automation with high reliability. The i.MX 8M Plus is a powerful quad Arm® Cortex®-A53 processor with speed up to 1.8 GHz integrated with a NPU of 2.3 TOPS that greatly accelerates machine learning inference. The vision engine is composed of two camera inputs and a HDR-capable Image Signal Processor (ISP).

Key features of i.MX 8M Plus

- Quard Arm® Cortex®-A53 core, up to 1.8 GHz
- Cortex®-M7 up to 800 MHz
- Neural Processing Unit (NPU)
- Dual Image Signal Processor and 1080p60 video encode/decode
- VIVANTE GC7000UL 3D GPU / GC520L 2D GPU
- ARM® TrustZone® support



2.4. CPU Variant Selection

The i.MX 8M Plus family offers a wide range of compatible CPU variants. To facilitate the decision guidance, the selection guide has been extended:

Feature	IMX8ML8	IMX8ML6	IMX8ML5	IMX8ML4	IMX8ML3	IMX8ML2
ARM® Cortex®-A53	Quad	Quad	Quad	Quad	Dual	Dual
VPU	Yes	Yes	Yes	No	Yes	Yes
NPU	Yes	No	Yes	No	Yes	Yes
ISP	Yes	Yes	No	No	Yes	No
HiFi 4	Yes	No	No	No	Yes	No

IMX8MLx-	Temperature range	Speed
DVNLZ	consumer	1.8 GHz
CVNKZ	industrial	1.6 GHz

For further information regarding the i.MX 8M Plus CPU, please visit the homepage of NXP.
NXP i.MX 8M Plus

2.5. Decision guidance byteENGINE IMX8MP

The following four steps help identifying the suitable byteENGINE for the specific customer application.

> Step 1: Select the needed CPU

> **Choose Options as described in CPU Variant Selection**

> Step 2: Select the needed flash memory type and capacity

> **Choose eMMC 8 / 16 / 32 / 64 / 128 GB**

> Step 3: Select the needed RAM capacity

> **Choose 512 / 1024 / 1536 / 2048 / 4096 / 8192 MB**

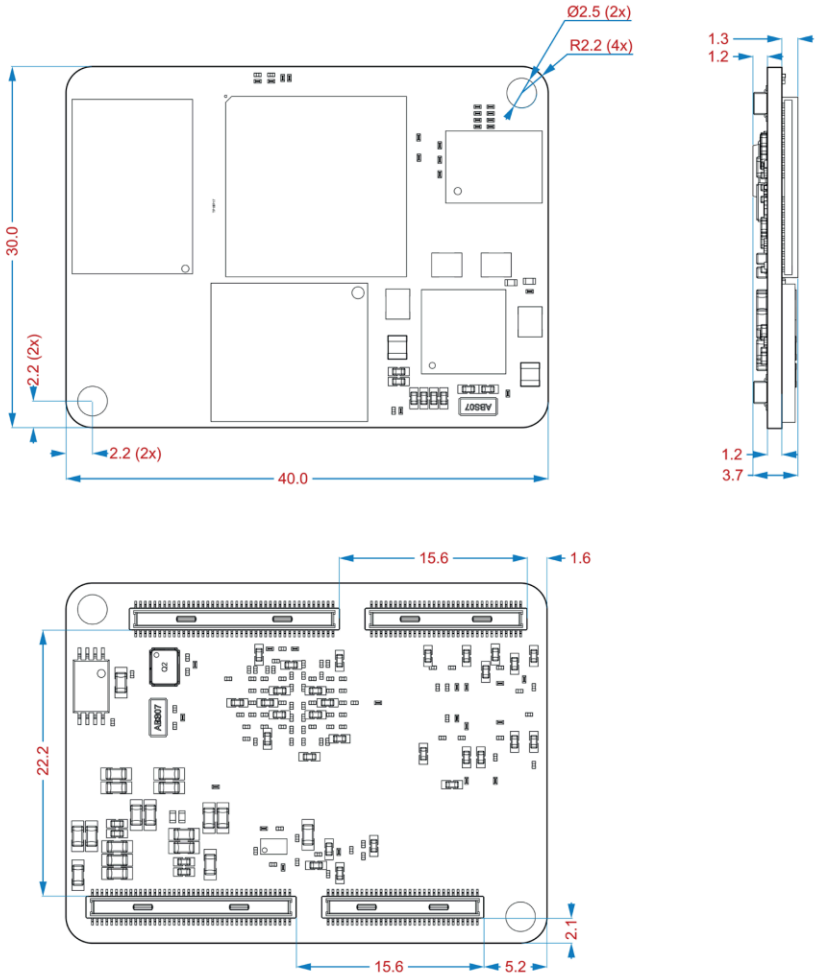
> Step 4: Select the needed temperature range

> **Choose consumer or industrial**

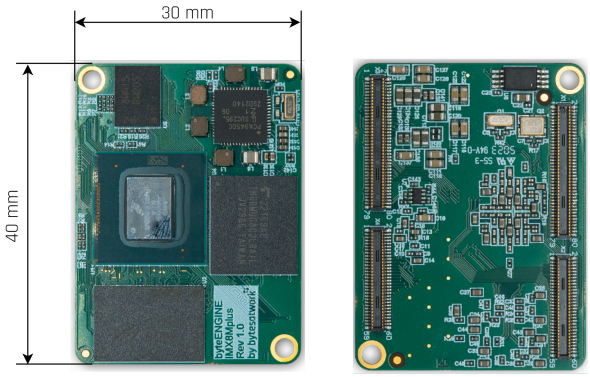
2.6. Dimensions of byteENGINE IMX8MP

The following illustration shows all important dimensions for mounting and installation of the industrial computing module byteENGINE IMX8MP.

> All dimensions are indicated in millimetres (mm)

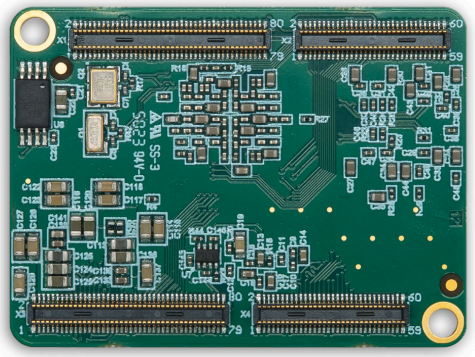


> Module design in scale 1:1:



2.7. byteENGINE IMX8MP connector layout

The IMX8MP is connected to the carrier board with 2x 80 and 2x 60 pins on four module connectors. The following picture shows the location of the connectors on the bottom side of the SOM byteENGINE.



Connectors

X1	DSI, CSI, PCIE, NCVV, LVDS
X2	USB, UART, I2C, SPI, PWM, SDMMC, SPDIF
X3	Ethernet, SDMMC, UART, I2C, PWM, PDM, SPDIF, SAI
X4	HDMI, Ethernet, UART, I2C, CAN, PWM, PDM, SAI

Schematic of the connectors X1, X2, X3 and X4

NOTICE

This module is held in the connectors with a considerable retention force. To avoid damaging the modules' connectors as well as the carrier board connectors while removing the module the use of an extraction tool is strongly recommended.

2.8. Connectors - DF40C-80DP and DF40C-60DP

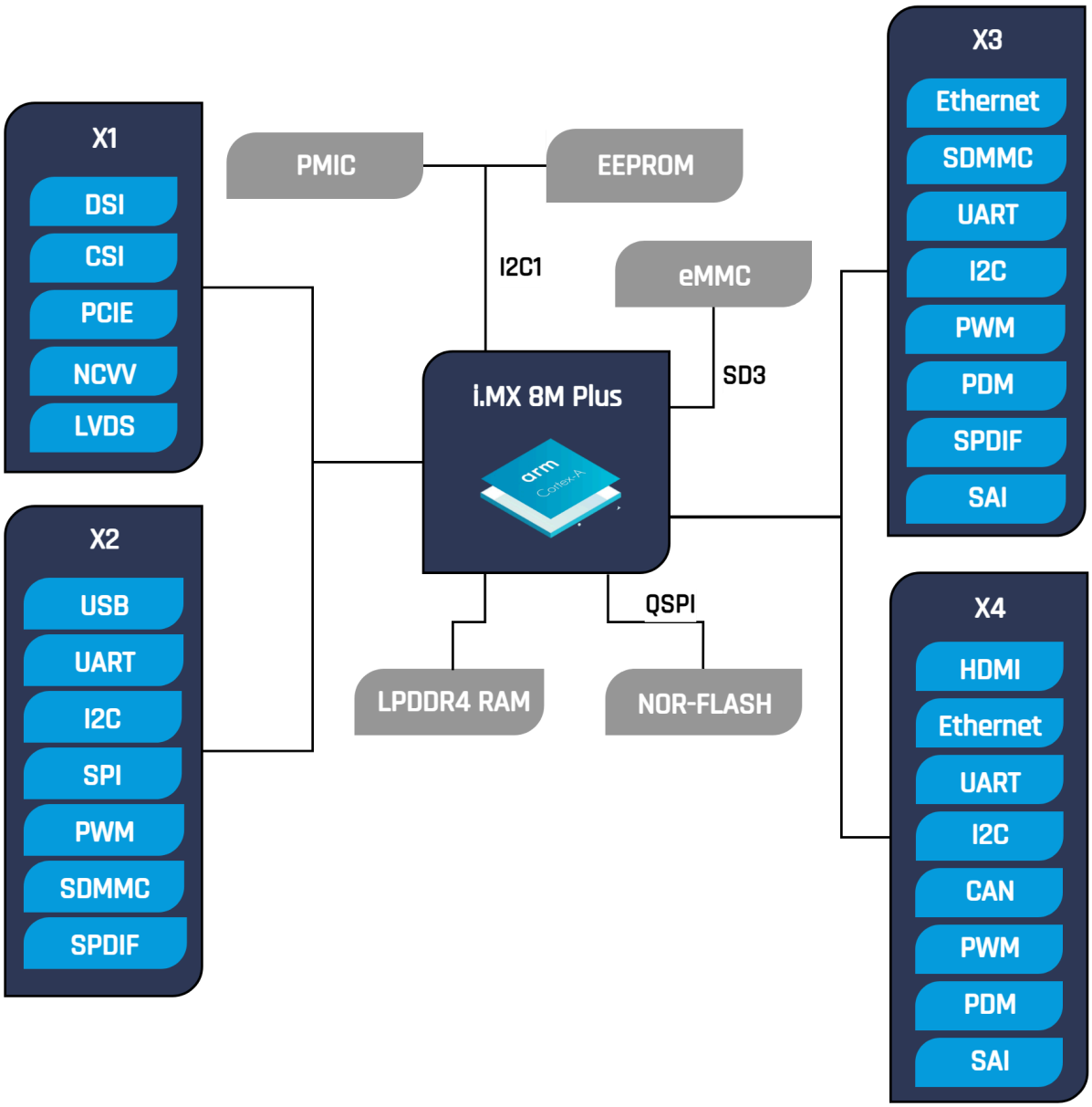
The byteENGINE uses four Hirose 0,4mm Board to Board Plug connectors. For more specific information about the connectors used, please consult the datasheet of the manufacturer.

Connectors	
X1, X3	DF40HC(3.0)-80DS-0.4V(51)
X2, X4	DF40HC(3.0)-60DS-0.4V(51)

Hirose DF40-Series Connectors

2.9. byteENGINE IMX8MP Connectors Overview

The following illustration shows the „Default-Configuration" of the byteENGINE IMX8MP. The function of the components shown in gray squares cannot be changed. The blue squares show the module connectors X1, X2, X3 and X4. The functions of X1, X2, X3 and X4 can be adapted and each connector module serves multiple functions. The detailed pinout-functions are shown in chapter 3. Pinout functions.



2.10. Configuration Tool for i.MX processors

The **Config Tools for i.MX** is a suite of evaluation and configuration tools that help users from initial evaluation to production software development. Config Tools for i.MX is an easy-to-use way to configure the pins and DDR of the i.MX processor devices.

The Config Tools for i.MX is installed as a desktop tool which then loads additional device information through a network connection, but does otherwise not need internet connection. It does not require a project setup, as all the settings are stored in text and generated source files, which then can be easily stored in a version control system or exchanged with other users.

The Pins Tool makes pin configuration easier and faster with an intuitive and easy user interface, which then generates normal C code that can then be used in any C and C++ application. The Pins Tool configures pin signals from multiplexing (muxing) to the electrical properties of pins, and it also creates Device Tree Snippets Include (.dtsi) files and reports in CSV format.

The DDR tool provides two main functionalities: configuration and validation

The DDR configuration provides a user-friendly graphical interface to configure the DDR controller and the DDR PHY. It can be used for tweaking some of the configuration parameters when you want to use different memory modules than the ones received with the board or when you want to optimize the configuration. DDR validation provides different scenarios to verify the DDR performance, by downloading a test image to the processor's internal RAM through a USB connection. The result is sent to the DDR tool via the UART. DDR validation can help verify DDR stability on the board in a non-OS environment.

i.MX Config Tool

NOTICE

Follow the link to i.MX Config Tool below. You need to install the Tool, then chose the processor.

3. Pinout functions

This chapter provides all relevant information for connecting and configuring the byteENGINE IMX8MP on a carrier board, including pin functions, available alternatives, restrictions, signal propagation delay, power supply and boot modes.

3.1. Restrictions

The following peripherals are internally connected to components on the module. They must not be used for external functions on the carrier board when the corresponding on-module components are populated and in use.

Restricted peripherals

I2C1	PMIC and EEPROM
SD3	eMMC
QUADSPI	NOR Flash

Ball	Pin Name	Used for
T29	NAND_CE1_B	eMMC
P28	NAND_CE2_B	eMMC
N28	NAND_CE3_B	eMMC
M28	NAND_CLE	eMMC
P29	NAND_DATA04	eMMC
N29	NAND_DATA05	eMMC
M29	NAND_DATA06	eMMC
R29	NAND_DATA07	eMMC
R26	NAND_DQS	eMMC
R28	NAND_RE_B	eMMC
T28	NAND_READY_B	eMMC
U28	NAND_WE_B	eMMC
U29	NAND_WP_B	eMMC

B6	GPI01_IO02	PMIC
D6	GPIO1_IO03	PMIC
E6	GPIO1_IO04	PMIC
F22	PMIC_ON_REQ	PMIC
J24	PMIC_STBY_REQ	PMIC
J29	POR_B	PMIC
AC8	I2C1_SCL	PMIC & EEPROM
AH7	I2C1_SDA	PMIC & EEPROM
N25	NAND_ALE	SPI_NOR
L26	NAND_CE0_B	SPI_NOR
R25	NAND_DATA00	SPI_NOR
L25	NAND_DATA01	SPI_NOR
L24	NAND_DATA02	SPI_NOR
N24	NAND_DATA03	SPI_NOR

3.2. Carrier board connector X1

Con	Pin	BGA Ball	Pin Name	Pin Function / Mode-Mux
				GPIOx / Dedicated function
X1	**1**		GND	
X1	**2**		GND	
X1	**3**	G22	ONOFF	SNVS_ONOFF
X1	**4**	C29	LVDS1_D3_P	LVDS1_D3_P
X1	**5**	G10	BOOT_MODE0	BOOT_MODE(0)
X1	**6**	D28	LVDS1_D3_N	LVDS1_D3_N
X1	**7**	F8	BOOT_MODE1	BOOT_MODE(1)
X1	**8**	B29	LVDS1_D2_P	LVDS1_D2_P
X1	**9**	G8	BOOT_MODE2	BOOT_MODE(2)
X1	**10**	C28	LVDS1_D2_N	LVDS1_D2_N
X1	**11**	G12	BOOT_MODE3	BOOT_MODE(3)
X1	**12**	A28	LVDS1_CLK_P	LVDS1_CLK_P
X1	**13**		GND	
X1	**14**	B28	LVDS1_CLK_N	LVDS1_CLK_N
X1	**15**	H29	LVDS0_D3_P	LVDS0_D3_P
X1	**16**	A26	LVDS1_D0_P	LVDS1_D0_P
X1	**17**	J28	LVDS0_D3_N	LVDS0_D3_N
X1	**18**	B26	LVDS1_D0_N	LVDS1_D0_N

Con	Pin	BGA Ball	Pin Name	Pin Function / Mode-Mux
				GPIOx / Dedicated function
X1	19	G29	LVDS0_D2_P	LVDS0_D2_P
X1	20	A27	LVDS1_D1_P	LVDS1_D1_P
X1	21	H28	LVDS0_D2_N	LVDS0_D2_N
X1	22	B27	LVDS1_D1_N	LVDS1_D1_N
X1	23	F29	LVDS0_CLK_P	LVDS0_CLK_P
X1	24		GND	
X1	25	G28	LVDS0_CLK_N	LVDS0_CLK_N
X1	26	A20	MIPI_DSI1_D3_P	MIPI_DSI1_D3_P
X1	27	E29	LVDS0_D1_P	LVDS0_D1_P
X1	28	B20	MIPI_DSI1_D3_N	MIPI_DSI1_D3_N
X1	29	F28	LVDS0_D1_N	LVDS0_D1_N
X1	30	A19	MIPI_DSI1_D2_P	MIPI_DSI1_D2_P
X1	31	D29	LVDS0_D0_P	LVDS0_D0_P
X1	32	B19	MIPI_DSI1_D2_N	MIPI_DSI1_D2_N
X1	33	E28	LVDS0_D0_N	LVDS0_D0_N
X1	34	A18	MIPI_DSI1_CLK_P	MIPI_DSI1_CLK_P
X1	35		GND	
X1	36		MIPI_DSI1_CLK_N	MIPI_DSI1_CLK_N
X1	37	A25	MIPI_CSI2_D0_P	MIPI_CSI2_D0_P
X1	38	A17	MIPI_DSI1_D1_P	MIPI_DSI1_D1_P
X1	39	B25	MIPI_CSI2_D0_N	MIPI_CSI2_D0_N
X1	40	B17	MIPI_DSI1_D1_N	MIPI_DSI1_D1_N
X1	41	A24	MIPI_CSI2_D1_P	MIPI_CSI2_D1_P
X1	42	A16	MIPI_DSI1_D0_P	MIPI_DSI1_D0_P
X1	43	B24	MIPI_CSI2_D1_N	MIPI_CSI2_D1_N
X1	44	B16	MIPI_DSI1_D0_N	MIPI_DSI1_D0_N
X1	45	A23	MIPI_CSI2_CLK_P	MIPI_CSI2_CLK_P
X1	46		GND	
X1	47	B23	MIPI_CSI2_CLK_N	MIPI_CSI2_CLK_N
X1	48	K28	CLKIN1	NVCC.CLKIN1
X1	49	A22	MIPI_CSI2_D2_P	MIPI_CSI2_D2_P
X1	50	L28	CLKIN2	NVCC.CLKIN2
X1	51	B22	MIPI_CSI2_D2_N	MIPI_CSI2_D2_N
X1	52	K29	CLKOUT1	NVCC.CLKOUT1
X1	53	A21	MIPI_CSI2_D3_P	MIPI_CSI2_D3_P
X1	54	L29	CLKOUT2	NVCC.CLKOUT2
X1	55	B21	MIPI_CSI2_D3_N	MIPI_CSI2_D3_N

Con	Pin	BGA Ball	Pin Name	Pin Function / Mode-Mux
				GPIOx / Dedicated function
X1	56		GND	
X1	57		GND	
X1	58		NC	
X1	59	D26	MIPI_CSI1_D3_P	MIPI_CSI1_D3_P
X1	60		GND	
X1	61	E26	MIPI_CSI1_D3_N	MIPI_CSI1_D3_N
X1	62	D16	PCIE_REF_PAD_CLK_P	PCIE_CLK_P
X1	63	D24	MIPI_CSI1_D2_P	MIPI_CSI1_D2_P
X1	64	E16	PCIE_REF_PAD_CLK_N	PCIE_CLK_N
X1	65	E24	MIPI_CSI1_D2_N	MIPI_CSI1_D2_N
X1	66		GND	
X1	67	D22	MIPI_CSI1_CLK_P	MIPI_CSI1_CLK_P
X1	68	A15	PCIE_TXN_P	PCIE_TXN_P
X1	69	E22	MIPI_CSI1_CLK_N	MIPI_CSI1_CLK_N
X1	70	B15	PCIE_TXN_N	PCIE_TXN_N
X1	71	D20	MIPI_CSI1_D1_P	MIPI_CSI1_D1_P
X1	72		GND	
X1	73	E20	MIPI_CSI1_D1_N	MIPI_CSI1_D1_N
X1	74	A14	PCIE_RXN_P	PCIE_RXN_P
X1	75	D18	MIPI_CSI1_D0_P	MIPI_CSI1_D0_P
X1	76	B14	PCIE_RXN_N	PCIE_RXN_N
X1	77	E18	MIPI_CSI1_D0_N	MIPI_CSI1_D0_N
X1	78		NC	
X1	79		GND	
X1	80		GND	

3.3. Carrier board connector X2

Con	Pin	BGA Ball	Pin Name	Pin Function / Mode-Mux							
				GPIOx / Dedicated function	1	2	3	4	5	6	7
X2	1		GND								
X2	2		GND								
X2	3	AD6	UART1_RXD	GPIO5_IO22	UART1_RX	UART1_TX	ECSPI3_SCLK				
X2	4	D12	USB2_VBUS	USB2_VBUS							
X2	5	AJ3	UART1_TXD	GPIO5_IO23	UART1_TX	UART1_RX	ECSPI3_MOSI				
X2	6	D8	USB2_ID	GPIO1_IO11	USB2_ID	PWM2_OUT	USDHC3_VSELECT	CCM_PMIC_READY			
X2	7	AE6	UART3_RXD	GPIO5_IO26	UART3_RX	UART3_TX	UART1_CTS_B	UART1_RTS_B	USDHC3_RESET_B	CAN2_TX	GPT1_CAPTURE2
X2	8	A4	USB2_PWR	GPIO1_IO14	USB2_PWR	PWM3_OUT	USDHC3_CD_B	CCM_CLKO1			
X2	9	AJ4	UART3_TXD	GPIO5_IO27	UART3_TX	UART3_RX	UART1_RTS_B	UART1_CTS_B	USDHC3_VSELECT	CAN2_RX	GPT1_CLK
X2	10	B5	USB2_OC	GPIO1_IO15	USB2_OC	PWM4_OUT	USDHC3_WP	CCM_CLKO2			
X2	11		GND								
X2	12		GND								
X2	13	AF6	UART2_RXD	GPIO5_IO24	UART2_RX	UART2_TX	ECSPI3_MISO	GPT1_COMPARE3			
X2	14	E14	USB2_D_N	USB2_D_N							
X2	15	AH4	UART2_TXD	GPIO5_IO25	UART2_TX	UART2_RX	ECSPI3_SS0	GPT1_COMPARE2			
X2	16	D14	USB2_D_P	USB2_D_P							
X2	17	AJ5	UART4_RXD	GPIO5_IO28	UART4_RX	UART4_TX	UART2_CTS_B	UART2_RTS_B	I2C6_SCL	GPT1_COMPARE1	PCIE1_CLKREQ_B
X2	18		GND								
X2	19	AH5	UART4_TXD	GPIO5_IO29	UART4_TX	UART4_RX	UART2_RTS_B	UART2_CTS_B	I2C6_SDA	GPT1_CAPTURE1	
X2	20	B13	USB2_TX_N	USB2_TX_N							
X2	21		GND								

Con	Pin	BGA Ball	Pin Name	Pin Function / Mode-Mux							
				GPIOx / Dedicated function	1	2	3	4	5	6	7
X2	22	A13	USB2_TX_P	USB2_TX_P							
X2	23	AC18	SPDIF_EXT_CLK	GPIO5_IO5	SPDIF1_EXT_CLK	PWM1_OUT	GPT1_COMPARE3				
X2	24		GND								
X2	25	AD18	SPDIF_RX	GPIO5_IO4	SPDIF1_IN	PWM2_OUT	I2C5_SDA	CAN1_RX	GPT1_COMPARE2		
X2	26	B12	USB2_RX_N	USB2_RX_N							
X2	27	AE18	SPDIF_TX	GPIO5_IO3	SPDIF1_OUT	PWM3_OUT	I2C5_SCL	CAN1_TX	GPT1_COMPARE1		
X2	28	A12	USB2_RX_P	USB2_RX_P							
X2	29		GND								
X2	30		GND								
X2	31	G18	JTAG_TCK	JTAG_TCK							
X2	32	A11	USB1_VBUS	USB1_VBUS							
X2	33	G14	JTAG_TMS	JTAG_TMS							
X2	34	B7	USB1_ID	GPIO1_IO10	USB1_ID	PWM3_OUT					
X2	35	G16	JTAG_TDI	JTAG_TDI							
X2	36	A5	USB1_PWR	GPIO1_IO12	USB1_PWR	SDMA2_EXT_EVENT1					
X2	37	F14	JTAG_TDO	JTAG_TDO							
X2	38	A6	USB1_OC	GPIO1_IO13	USB1_OC	PWM2_OUT					
X2	39	G20	JTAG_MOD	JTAG_MOD							
X2	40		GND								
X2	41		GND								
X2	42	E10	USB1_D_N	USB1_D_N							
X2	43	A7	GPIO1_IO00	GPIO1_IO00	ISP_FL_TRIG_0	CCM_ENET_PHY_REF_CLK	CCM_REF_CLK_32K	CCM_EXT_CLK1			
X2	44	D10	USB1_D_P	USB1_D_P							
X2	45	E8	GPIO1_IO01	GPIO1_IO01	ISP_SHUTTER_TRIG_0	PWM1_OUT	CCM_REF_CLK_24M	CCM_EXT_CLK2			

Con	Pin	BGA Ball	Pin Name	Pin Function / Mode-Mux							
				GPIOx / Dedicated function	1	2	3	4	5	6	7
X2	46		GND								
X2	47	B4	GPIO1_IO05	GPIO1_IO05	ISP_FL_TRIG_1	CCM_PMIC_READY	M7_NMI				
X2	48	B10	USB1_TX_N	USB1_TX_N							
X2	49	A3	GPIO1_IO06	GPIO1_IO06	ISP_SHUTTER_TRIG_1	ENET_QOS_MDC	USDHC1_CD_B	CCM_EXT_CLK3			
X2	50	A10	USB1_TX_P	USB1_TX_P							
X2	51	F6	GPIO1_IO07	GPIO1_IO07	ISP_FLASH_TRIG_1	ENET_QOS_MDIO	USDHC1_WP	CCM_EXT_CLK4			
X2	52		GND								
X2	53	A8	GPIO1_IO08	GPIO1_IO08	ISP_PRELIGHT_TRIG_1	PWM1_OUT	USDHC2_RESET_B	ENET_QOS_1588_EVENT0_AUX_IN	ENET_QOS_1588_EVENT0_IN		
X2	54	B9	USB1_RX_N	USB1_RX_N							
X2	55	B8	GPIO1_IO09	GPIO1_IO09	ISP_SHUTTER_OPEN_1	PWM2_OUT	USDHC3_RESET_B	ENET_QOS_1588_EVENT0_OUT	SDMA2_EXT_EVENT0		
X2	56	A9	USB1_RX_P	USB1_RX_P							
X2	57		SYS_nRESET								
X2	58		NC								
X2	59		GND								
X2	60		GND								

3.4. Carrier board connector X3

Con	Pin	BGA Ball	Pin Name	Pin Function / Mode-Mux							
				GPIOx / Dedicated function	1	2	3	4	5	6	7
X3	1		VSYS								
X3	2		VSYS								
X3	3		VSYS								
X3	4		VSYS								
X3	5		VSYS								
X3	6		VSYS								
X3	7		VSYS								
X3	8		VSYS								
X3	9		VSYS								
X3	10		VSYS								
X3	11		GND								
X3	12		GND								
X3	13		GND								
X3	14		GND								
X3	15		GND								
X3	16		GND								
X3	17	AB29	SD2_CLK	GPIO2_IO13	USDHC2_CLK	UART4_TX	UART4_RX	ECSPI2_SCLK			
X3	18	AH28	ENET_MDC	GPIO1_IO16	ENET_QOS_MDC	USDHC3_STROBE	SAI6_TX_DATA0				
X3	19	AB28	SD2_CMD	GPIO2_IO14	USDHC2_CMD	UART4_RX	UART4_TX	ECSPI2_MOSI	PDM_CLK		
X3	20	AH29	ENET_MDIO	GPIO1_IO17	ENET_QOS_MDIO	USDHC3_DATA5	SAI6_TX_SYNC	PDM_BIT_STREAM3			
X3	21	AC28	SD2_DATA0	GPIO2_IO15	USDHC2_DATA0	UART2_RX	UART2_TX	I2C4_SDA	PDM_BIT_STREAM0		

Con	Pin	BGA Ball	Pin Name	Pin Function / Mode-Mux							
				GPIOx / Dedicated function	1	2	3	4	5	6	7
X3	22	AF24	ENET_TX_CTL	GPIO1_IO22	ENET_QOS_RGMII_TX_CTL	USDHC3_DATA0	SAI6_MCLK	SPDIF1_OUT			
X3	23	AC29	SD2_DATA1	GPIO2_IO16	USDHC2_DATA1	UART2_TX	UART2_RX	I2C4_SCL	PDM_BIT_STREAM1		
X3	24	AE24	ENET_TXC	GPIO1_IO23	ENET_QOS_RGMII_TXC	USDHC3_DATA1	SAI7_TX_DATA0	ENET_QOS_TX_ER			
X3	25	AA26	SD2_DATA2	GPIO2_IO17	USDHC2_DATA2	ECSPI2_SS0	PDM_BIT_STREAM2	SPDIF1_OUT			
X3	26	AC25	ENET_TD0	GPIO1_IO21	ENET_QOS_RGMII_TD0	USDHC3_WP	SAI6_RX_BCLK	PDM_CLK			
X3	27	AA25	SD2_DATA3	GPIO2_IO18	USDHC2_DATA3	ECSPI2_MISO	PDM_BIT_STREAM3	SPDIF1_IN			
X3	28	AE26	ENET_TD1	GPIO1_IO20	ENET_QOS_RGMII_TD1	USDHC3_CD	SAI6_RX_SYNC	PDM_BIT_STREAM0			
X3	29	AD29	SD2_CD_B	GPIO2_IO12	USDHC2_CD_B						
X3	30	AF26	ENET_TD2	GPIO1_IO19	ENET_QOS_RGMII_TD2	USDHC3_DATA7	SAI6_RX_DATA0	PDM_BIT_STREAM1	ENET_QOS_TX_CLK		
X3	31	AC26	SD2_WP	GPIO2_IO20	USDHC2_WP	CORESIGHT_EVENTI					
X3	32	AD24	ENET_TD3	GPIO1_IO18	ENET_QOS_RGMII_TD3	USDHC3_DATA6	SAI6_TX_BCLK	PDM_BIT_STREAM2			
X3	33	AD28	SD2_RESET_B	GPIO2_IO19	USDHC2_RESET_B						
X3	34	AE28	ENET_RX_CTL	GPIO1_IO24	ENET_QOS_RGMII_RX_CTL	USDHC3_DATA2	SAI7_TX_SYNC	PDM_BIT_STREAM3			
X3	35	W28	SD1_CLK	GPIO2_IO0	USDHC1_CLK	UART1_TX	UART1_RX	I2C5_SCL	ENET1_MDC		
X3	36	AE29	ENET_RXC	GPIO1_IO25	ENET_QOS_RGMII_RXC	USDHC3_DATA3	SAI7_TX_BCLK	PDM_BIT_STREAM2	ENET_QOS_RX_ER		
X3	37	W29	SD1_CMD	GPIO2_IO1	USDHC1_CMD	UART1_RX	UART1_TX	I2C5_SDA	ENET1_MDIO		
X3	38	AG29	ENET_RD0	GPIO1_IO26	ENET_QOS_RGMII_RD0	USDHC3_DATA4	SAI7_RX_DATA0	PDM_BIT_STREAM1			
X3	39	Y29	SD1_DATA0	GPIO2_IO2	USDHC1_DATA0	UART1_CTS_B	UART1_RTS_B	I2C6_SCL	ENET1_RGMII_TD1		
X3	40	AG28	ENET_RD1	GPIO1_IO27	ENET_QOS_RGMII_RD1	USDHC3_RESET_B	SAI7_RX_SYNC	PDM_BIT_STREAM0			
X3	41		GND								
X3	42	AF29	ENET_RD2	GPIO1_IO28	ENET_QOS_RGMII_RD2	USDHC3_CLK	SAI7_RX_BCLK	PDM_CLK			
X3	43	Y28	SD1_DATA1	GPIO2_IO3	USDHC1_DATA1	UART1_RTS_B	UART1_CTS_B	I2C6_SDA	ENET1_RGMII_TD0		
X3	44	AF28	ENET_RD3	GPIO1_IO29	ENET_QOS_RGMII_RD3	USDHC3_CMD	SAI7_MCLK	SPDIF1_IN			
X3	45	V29	SD1_DATA2	GPIO2_IO4	USDHC1_DATA2	UART2_TX	UART2_RX	I2C4_SCL	ENET1_RGMII_RD0		
X3	46		GND								

Con	Pin	BGA Ball	Pin Name	Pin Function / Mode-Mux							
				GPIOx / Dedicated function	1	2	3	4	5	6	7
X3	47	V28	SD1_DATA3	GPIO2_IO5	USDHC1_DATA3	UART2_RX	UART2_TX	I2C4_SDA	ENET1_RGMII_RD1		
X3	48	AE20	ECSPI1_SS0	GPIO5_IO9	ECSPI1_SS0	UART3_RTS_B	UART3_CTS_B	I2C2_SDA	SAI7_TX_SYNC		
X3	49	U26	SD1_DATA4	GPIO2_IO6	USDHC1_DATA4	UART2_RTS_B	UART2_CTS_B	I2C1_SCL	ENET1_RGMII_TX_CTL		
X3	50	AC20	ECSPI1_MOSI	GPIO5_IO7	ECSPI1_MOSI	UART3_TX	UART3_RX	I2C1_SDA	SAI7_RX_BCLK		
X3	51	AA29	SD1_DATA5	GPIO2_IO7	USDHC1_DATA5	UART2_CTS_B	UART2_RTS_B	I2C1_SDA	ENET1_TX_ER		
X3	52	AD20	ECSPI1_MISO	GPIO5_IO8	ECSPI1_MISO	UART3_CTS_B	UART3_RTS_B	I2C2_SCL	SAI7_RX_DATA0		
X3	53	AA28	SD1_DATA6	GPIO2_IO8	USDHC1_DATA6	UART3_TX	UART3_RX	I2C2_SCL	ENET1_RGMII_RX_CTL		
X3	54	AF20	ECSPI1_SCLK	GPIO5_IO6	ECSPI1_SCLK	UART3_RX	UART3_TX	I2C1_SCL	SAI7_RX_SYNC		
X3	55	U25	SD1_DATA7	GPIO2_IO9	USDHC1_DATA7	UART3_RX	UART3_TX	I2C2_SDA	ENET1_RX_ER		
X3	56		GND								
X3	57	W25	SD1_RESET_B	GPIO2_IO10	USDHC1_RESET_B	UART3_RTS_B	UART3_CTS_B	I2C3_SCL	ENET1_TX_CLK		
X3	58	AJ22	ECSPI2_SS0	GPIO5_IO13	ECSPI2_SS0	UART4_RTS_B	UART4_CTS_B	I2C4_SDA	CCM_CLKO2		
X3	59	W26	SD1_STROBE	GPIO2_IO11	USDHC1_STROBE	UART3_CTS_B	UART3_RTS_B	I2C3_SDA			
X3	60	AJ21	ECSPI2_MOSI	GPIO5_IO11	ECSPI2_MOSI	UART4_TX	UART4_RX	I2C3_SDA	SAI7_TX_DATA0		
X3	61		VSELECT								
X3	62	AH20	ECSPI2_MISO	GPIO5_IO12	ECSPI2_MISO	UART4_CTS_B	UART4_RTS_B	I2C4_SCL	SAI7_MCLK	CCM_CLKO1	
X3	63		VMMC								
X3	64	AH21	ECSPI2_SCLK	GPIO5_IO10	ECSPI2_SCLK	UART4_RX	UART4_TX	I2C3_SCL	SAI7_TX_BCLK		
X3	65		VDD_IO								
X3	66		GND								
X3	67		NVCC_SD2								
X3	68	AJ20	SAI3_MCLK	GPIO5_IO2	SAI3_MCLK	SAI5_MCLK	PWM4_OUT	SPDIF1_IN	SPDIF1_OUT		
X3	69		NC								
X3	70	AC16	SAI3_TXFS	GPIO4_IO31	SAI3_TX_SYNC	SAI2_TX_DATA1	SAI3_TX_DATA1	SAI5_RX_DATA1	UART2_TX	UART2_RX	PDM_BIT_STREAM3
X3	71		GND								

Con	Pin	BGA Ball	Pin Name	Pin Function / Mode-Mux							
				GPIOx / Dedicated function	1	2	3	4	5	6	7
X3	72	AH19	SAI3_TXC	GPIO5_IO0	SAI3_TX_BCLK	SAI2_TX_DATA2	SAI5_RX_DATA2	GPT1_CAPTURE1	UART2_RX	UART2_TX	PDM_BIT_STREAM2
X3	73	AH23	EARC_AUX	EARC_AUX							
X3	74	AH18	SAI3_TXD	GPIO5_IO1	SAI3_TX_DATA0	SAI2_TX_DATA3	SAI5_RX_DATA3	GPT1_CAPTURE2	SPDIF1_EXT_CLK		
X3	75	AH22	EARC_N_HPD	EARC_N_HPD							
X3	76	AJ19	SAI3_RXFS	GPIO4_IO28	SAI3_RX_SYNC	SAI2_RX_DATA1	SAI3_RX_DATA1	SAI5_RX_SYNC	SPDIF1_IN	PDM_BIT_STREAM0	
X3	77	AJ23	EARC_P_UTIL	EARC_P_UTIL							
X3	78	AJ18	SAI3_RXC	GPIO4_IO29	SAI3_RX_BCLK	SAI2_RX_DATA2	SAI5_RX_BCLK	GPT1_CLK	UART2_CTS_B	UART2_RTS_B	PDM_CLK
X3	79		GND								
X3	80	AF18	SAI3_RXD	GPIO4_IO30	SAI3_RX_DATA0	SAI2_RX_DATA3	SAI5_RX_DATA0	PDM_BIT_STREAM1	UART2_CTS_B	UART2_RTS_B	

3.5. Carrier board connector X4

Con	Pin	BGA Ball	Pin Name	Pin Function / Mode-Mux							
				GPIOx / Dedicated function	1	2	3	4	5	6	7
X4	1		GND								
X4	2	AJ15	SAI2_MCLK	GPIO4_IO27	SAI2_MCLK	SAI3_MCLK	SAI5_MCLK	ENET_QOS_1588_EVENT3_IN	ENET_QOS_1588_EVENT3_AUX_IN	CAN2_RX	
X4	3	AC22	HDMI_DDC_SCL	GPIO3_IO26	HDMI_SCL	I2C5_SCL	CAN1_TX				
X4	4	AJ17	SAI2_TXFS	GPIO4_IO24	SAI2_TX_SYNC	SAI2_TX_DATA1	SAI5_TX_DATA1	ENET_QOS_1588_EVENT3_OUT	UART1_RTS_B	UART1_CTS_B	PDM_BIT_STREAM2
X4	5	AF22	HDMI_DDC_SDA	GPIO3_IO27	HDMI_SDA	I2C5_SDA	CAN1_RX				
X4	6	AH15	SAI2_TXC	GPIO4_IO25	SAI2_TX_BCLK	SAI5_TX_DATA2	CAN1_RX	PDM_BIT_STREAM1			
X4	7	AE22	HDMI_HPD	GPIO3_IO29	HDMI_HPD	HDMI_HPD_O	I2C6_SDA	CAN2_RX			
X4	8	AH16	SAI2_TXD0	GPIO4_IO26	SAI2_TX_DATA0	SAI5_TX_DATA3	CAN2_TX	ENET_QOS_1588_EVENT2_IN	ENET_QOS_1588_EVENT2_AUX_IN		
X4	9	AD22	HDMI_CEC	GPIO3_IO28	HDMI_CEC	I2C6_SCL	CAN2_TX				
X4	10	AH17	SAI2_RXFS	GPIO4_IO21	SAI2_RX_SYNC	SAI2_RX_DATA1	SAI5_TX_SYNC	SAI5_TX_DATA1	UART1_TX	UART1_RX	PDM_BIT_STREAM2
X4	11		GND								
X4	12	AJ16	SAI2_RXC	GPIO4_IO22	SAI2_RX_BCLK	SAI5_TX_BCLK	CAN1_TX	PDM_BIT_STREAM1	UART1_RX	UART1_TX	
X4	13	AH27	HDMI_TX2_P	HDMI_TX2_P							
X4	14	AJ14	SAI2_RXD0	GPIO4_IO23	SAI2_RX_DATA0	SAI2_TX_DATA1	SAI5_TX_DATA0	ENET_QOS_1588_EVENT2_OUT	UART1_RTS_B	UART1_CTS_B	PDM_BIT_STREAM3
X4	15	AJ27	HDMI_TX2_N	HDMI_TX2_N							
X4	16		GND								
X4	17	AH26	HDMI_TX1_P	HDMI_TX1_P							
X4	18	AE12	SAI1_MCLK	GPIO4_IO20	SAI1_MCLK	SAI1_TX_BCLK	ENET1_TX_CLK				

Con	Pin	BGA Ball	Pin Name	Pin Function / Mode-Mux							
				GPIOx / Dedicated function	1	2	3	4	5	6	7
X4	19	AJ26	HDMI_TX1_N	HDMI_TX1_N							
X4	20	AF12	SAI1_TXFS	GPIO4_IO10	SAI1_TX_SYNC	ENET1_RGMII_RX_CTL					
X4	21	AH25	HDMI_TX0_P	HDMI_TX0_P							
X4	22	AJ12	SAI1_TXC	GPIO4_IO11	SAI1_TX_BCLK	ENET1_RGMII_RXC					
X4	23	AJ25	HDMI_TX0_N	HDMI_TX0_N							
X4	24	AJ11	SAI1_TXD0	GPIO4_IO12	SAI1_TX_DATA0	ENET1_RGMII_TD0					
X4	25	AH24	HDMI_TXC_P	HDMI_TXC_P							
X4	26	AJ10	SAI1_TXD1	GPIO4_IO13	SAI1_TX_DATA1	ENET1_RGMII_TD1					
X4	27	AJ24	HDMI_TXC_N	HDMI_TXC_N							
X4	28	AH11	SAI1_TXD2	GPIO4_IO14	SAI1_TX_DATA2	ENET1_RGMII_TD2					
X4	29		GND								
X4	30	AD12	SAI1_TXD3	GPIO4_IO15	SAI1_TX_DATA3	ENET1_RGMII_TD3					
X4	31	AF14	SAI5_MCLK	GPIO3_IO25	SAI5_MCLK	SAI1_TX_BCLK	I2C5_SDA	PWM1_OUT	CAN2_RX		
X4	32	AH13	SAI1_TXD4	GPIO4_IO16	SAI1_TX_DATA4	ENET1_RGMII_TX_CTL	SAI6_RX_BCLK	SAI6_TX_BCLK			
X4	33	AC14	SAI5_RXFS	GPIO3_IO19	SAI5_RX_SYNC	SAI1_TX_DATA0	I2C6_SCL	PWM4_OUT			
X4	34	AH14	SAI1_TXD5	GPIO4_IO17	SAI1_TX_DATA5	ENET1_RGMII_TXC	SAI6_TX_DATA0	SAI6_RX_DATA0			
X4	35	AD14	SAI5_RXC	GPIO3_IO20	SAI5_RX_BCLK	SAI1_TX_DATA1	I2C6_SDA	PWM3_OUT	PDM_CLK		
X4	36	AC12	SAI1_TXD6	GPIO4_IO18	SAI1_TX_DATA6	ENET1_RX_ER	SAI6_RX_SYNC	SAI6_TX_SYNC			
X4	37	AE16	SAI5_RXD0	GPIO3_IO21	SAI5_RX_DATA0	SAI1_TX_DATA2	I2C5_SCL	PWM2_OUT	PDM_BIT_STREAM0		
X4	38	AJ13	SAI1_TXD7	GPIO4_IO19	SAI1_TX_DATA7	ENET1_TX_ER	SAI6_MCLK	PDM_CLK			
X4	39	AD16	SAI5_RXD1	GPIO3_IO22	SAI5_RX_DATA1	SAI1_TX_DATA3	SAI1_TX_SYNC	SAI5_TX_SYNC	PDM_BIT_STREAM1	CAN1_TX	
X4	40	AJ9	SAI1_RXFS	GPIO4_IO0	SAI1_RX_SYNC	ENET1_1588_EVENT0_IN					
X4	41	AF16	SAI5_RXD2	GPIO3_IO23	SAI5_RX_DATA2	SAI1_TX_DATA4	SAI1_TX_SYNC	SAI5_TX_BCLK	PDM_BIT_STREAM2	CAN1_RX	
X4	42	AH8	SAI1_RXC	GPIO4_IO1	SAI1_RX_BCLK	ENET1_1588_EVENT0_OUT	PDM_CLK				

Con	Pin	BGA Ball	Pin Name	Pin Function / Mode-Mux							
				GPIOx / Dedicated function	1	2	3	4	5	6	7
X4	43	AE14	SAI5_RXD3	GPIO3_IO24	SAI5_RX_DATA3	SAI1_TX_DATA5	SAI1_TX_SYNC	SAI5_TX_DATA0	PDM_BIT_STREAM3	CAN2_TX	
X4	44	AC10	SAI1_RXD0	GPIO4_IO2	SAI1_RX_DATA0	ENET1_1588_EVENT1_IN	SAI1_TX_DATA1	PDM_BIT_STREAM0			
X4	45		GND								
X4	46	AF10	SAI1_RXD1	GPIO4_IO3	SAI1_RX_DATA1	ENET1_1588_EVENT1_OUT	PDM_BIT_STREAM1				
X4	47	AH6	I2C2_SCL	GPIO5_IO16	I2C2_SCL	USDHC3_CD_B	ECSPI1_MISO	ENET_QOS_1588_EVENT1_IN	ENET_QOS_1588_EVENT1_AUX_IN		
X4	48	AH9	SAI1_RXD2	GPIO4_IO4	SAI1_RX_DATA2	ENET1_MDC	PDM_BIT_STREAM2				
X4	49	AE8	I2C2_SDA	GPIO5_IO17	I2C2_SDA	USDHC3_WP	ECSPI1_SS0	ENET_QOS_1588_EVENT1_OUT			
X4	50	AJ8	SAI1_RXD3	GPIO4_IO5	SAI1_RX_DATA3	ENET1_MDIO	PDM_BIT_STREAM3				
X4	51	AF8	I2C4_SCL	GPIO5_IO20	I2C4_SCL	PCIE1_CLKREQ_B	ECSPI2_MISO	PWM2_OUT			
X4	52	AD10	SAI1_RXD4	GPIO4_IO6	SAI1_RX_DATA4	ENET1_RGMII_RD0	SAI6_TX_BCLK	SAI6_RX_BCLK			
X4	53	AD8	I2C4_SDA	GPIO5_IO21	I2C4_SDA	ECSPI2_SS0	PWM1_OUT				
X4	54	AE10	SAI1_RXD5	GPIO4_IO7	SAI1_RX_DATA5	ENET1_RGMII_RD1	SAI6_TX_DATA0	SAI6_RX_DATA0	SAI1_RX_SYNC		
X4	55	AJ7	I2C3_SCL	GPIO5_IO18	I2C3_SCL	ECSPI2_SCLK	PWM4_OUT	GPT2_CLK			
X4	56	AH10	SAI1_RXD6	GPIO4_IO8	SAI1_RX_DATA6	ENET1_RGMII_RD2	SAI6_TX_SYNC	SAI6_RX_SYNC			
X4	57	AJ6	I2C3_SDA	GPIO5_IO19	I2C3_SDA	ECSPI2_MOSI	PWM3_OUT	GPT3_CLK			
X4	58	AH12	SAI1_RXD7	GPIO4_IO9	SAI1_RX_DATA7	ENET1_RGMII_RD3	SAI6_MCLK	SAI1_TX_SYNC	SAI1_TX_DATA4		
X4	59		GND								
X4	60		GND								

3.6. Signal Propagation Delay

The signal propagation delay table provides the relevant propagation delay values for module signals and supports timing analysis and carrier board design. For detailed signal propagation delay values, refer to the Signal Propagation Delay Table. These values should be considered when performing timing analysis and designing the carrier board.

Signal Propagation Delay Table for byteENGINE IMX8MP

3.7. Power Supply

- The byteENGINE can be powered with 3.3V to 5.5V.
- The recommended power supply is 5V.

PCA9450CHN Power Manage IC (PMIC) for i.MX 8M Plus

3.8. Boot Modes byteENGINE IMX8MP

The Module is designed to boot from SDCARD. If a valid u-boot is placed in NOR Flash it will boot from NOR. If a valid u-boot is present on SDCARD it always boots from SDCARD regardless of the content of the NOR Flash. The boot sequence can be redefined with OPT flashing

Datasheet i.MX 8M Plus

4. Ordering info

The Order Code allows customers to easily recognize the detailed specification of the ordered SOM. Please refer to chapter Decision guidance byteENGINE IMX8MP for further information.

byteENGINE-IMX8MP-[TYPE]-[SPEED]-[RAM]-[FLASH]-[temp-range]-[revision]

[TYPE]	**CPU type**	Comprehensive, see Additional information
[SPEED]	**Clock speed**	1.6 GHz / 1.8 GHz
[RAM]	**RAM size**	512 / 1024 / 1536 / 2048 / 4096 / 8192 MB
[FLASH]	**eMMC flash size**	8 / 16 / 32 / 64 / 128 GB
[temp-range]	**Temperature range**	[C] Consumer 0° to +85° C [I] Industrial -40°C to +85 °C
[revision]	**Revision**	1.1

5. References

NOTICE

Files can only be downloaded with login credentials. Please request your download credentials via support@bytesatwork.ch or contact your sales representative.

Links

Hardware Design

Schematic of the connectors X1, X2, X3, X4

Altium Schematic of the connectors X1, X2, X3, X4

Altium Library

STEP Model

Detailed pinout for byteENGINE IMX8MP

Signal Propagation Delay table for byteENGINE IMX8MP

Component Documentation

Hirose DF40-Series Connectors

NXP i.MX 8M Plus Family:

PCA9450CHN Power Manage IC (PMIC) for i.MX 8M Plus

Software & Configuration

NXP Config Tools for i.MX Application Processors

meta-bytesatwork on github

byteWIKI

bytesatwork

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