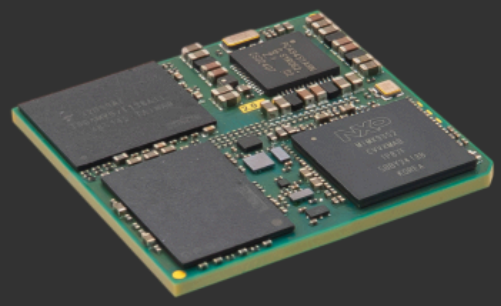
bytesatwork

DataSheet

Rev. 2.2 13.06.2025



industrial computing module

byteENGINE IMX9x

OSM-S

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Imprint

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Symbols and Typographic Conventions

These symbols represent important details or aspects for working with bytesatwork-products.

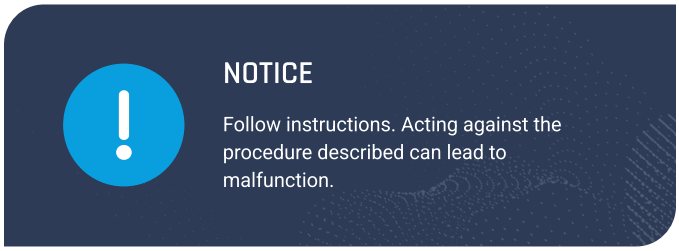

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Table of Contents

1. Revision History

Hardware Revision	Marking on PCB	Release Date	Info
2.1	Rev.2.1	Dec 2024	Modifications to adapt OSM-S Standard 1.2: Swap of Pins U15 and V15
2.0	Rev.2.0	July 2024	FLEXSPI1 available on SPI_A
1.0	Rev. 1.0	March 2024	First revision (sample)

NOTICE

This document refers to byteENGINE IMX9x Rev.2.1

2. Overview

2.1. General Information

The byteENGINE IMX9x is a high performance industrial oriented computing module. It allows you a short time-to-market, reducing development costs and substantial design risks.

The System on Module (SOM) uses the i.MX9 devices which are based on the high-performance dual core ARM® Cortex®-A55 64-bit RISC core operating at up to 1.7 GHz.

The devices of the i.MX93 family also embed a Cortex®-M33 32-bit RISC core operating at up to 250 MHz frequency.

The Cortex®-M33 core features a floating point unit (FPU) which supports ARM® single precision data-processing instructions and data types. Furthermore, the devices of the i.MX 9 family embed a micro Neural Processing Unit (NPU).

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2.2. Technical Data

Feature		Details
CPU	Architecture	Up to dual core Arm® Cortex®-A55 processors
	CPU	See Link for further information: Block diagram of IMX9x See NXP Homepage for further Information: i.MX 9x
	Cache	32KB L1 instruction Cache 32KB L1 Data Cache 64 kB per-core L2 Cache
	Frequency (max.)	Up to 1.7 GHz
	Floating Point	Floating Point Unit (FPU) with support of the Arm® VFPv4-D16 architecture
	Co-Processors	1x Cortex®-M33 CPU operating up to 2500 MHz 16KB System Cache, 16KB Code Cache, 256KB tightly coupled memory
	Security	Trustzone (TZ) architecture, Trusted Resource Domain Controller, Edge Lock
NPU	Neural Processing Unit	256MAC operating up to 16 GHz and 2 OPS/MAC > NPU targets 8-bit and 16-bit RNN > Handle 8-bit weights
ISI	Image Sensor Interface	200Mpixel/s ISP supporting up to 2K horizontal resolution
Memory on Chip	ORM /RAM	> Boot ROM (256 kb) for Cortex® A55 > Boot ROM (256 kb) for Cortex® M33 > On-Chip RAM (640 kb)
Memory External	DRAM	Up to 2 GB 16-bit LPDDR4X with inline ECC
	Flash	Up to 128 GB eMMC
Ethernet	Speed	1x 10/100/1000 Mbps & IEEE 1588 1x 10/100/1000 Mbps & IEEE 1588 with TSN
Multimedia	Pixel Pipeline (PXP)	> BitBit > Flexible image composition options > Porter-Duff Operation > Image rotation and resize > Color space conversion > Multiple pixel format support > Standard 2D-DMA operation
	LCDIF Display Controller	The LCDIF can drive any of these two > MIPI DSI: up to 1920x1200p60 And (depending on the byteENGINE IMX9x variant: > LVDS Tx: up to 1366x768p60 or 1280x800p60 or > Parallel display: up to 1366x768p60 or 1280x800p60
	MIPI CSI-2 Interface	> One 2-lane MIPI CSI-2 camera input

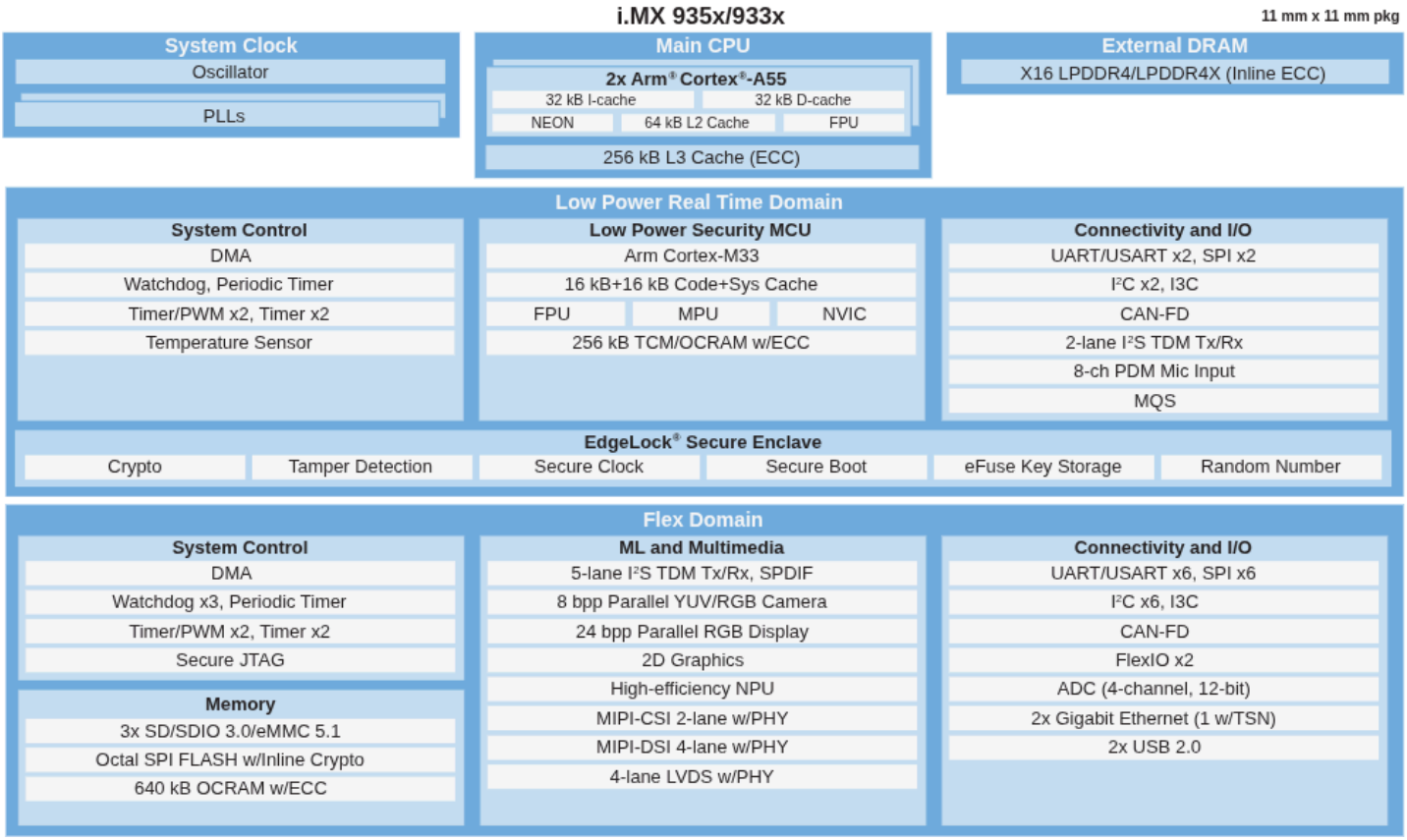
	Audio	> Three SAI interfaces > One SPDIF supports raw capture mode > 24-bit PDM supports up to 8 microphones (4-lanes)
Expansion	**SD/SDIO 3.0**	3
ADC	**Analog Digital Converter**	12-bit 4-channel ADC
USB	**USB 2.0**	2
Serial	**SPI**	Up to 8
	I2C	Up to 8
	UART	Up to 8
	OctalSPI	1
	FlexIO	2 32-pin
	CAN-FD	1
	I3C	2
Miscellaneous	**Watchdog**	5
	Secure JTAG	Yes
	GPIO (4 x 32 Bit)	128 GPIOs
	PWM / Timer	6 TPM (Timer / PWM Module)
	Boot Mode	Secure boot supported
	Temperature Probe	1
Mechanical information	**Input Voltage**	5.0 V
	Power Consumption	2 W
	Dimensions	30 x 30 mm
	Operating Temperature	> Industrial temperature range: -40 to +85° C > Consumer temperature range: 0 to +70° C
Operating System	**Linux**	meta-bytesatwork available on github

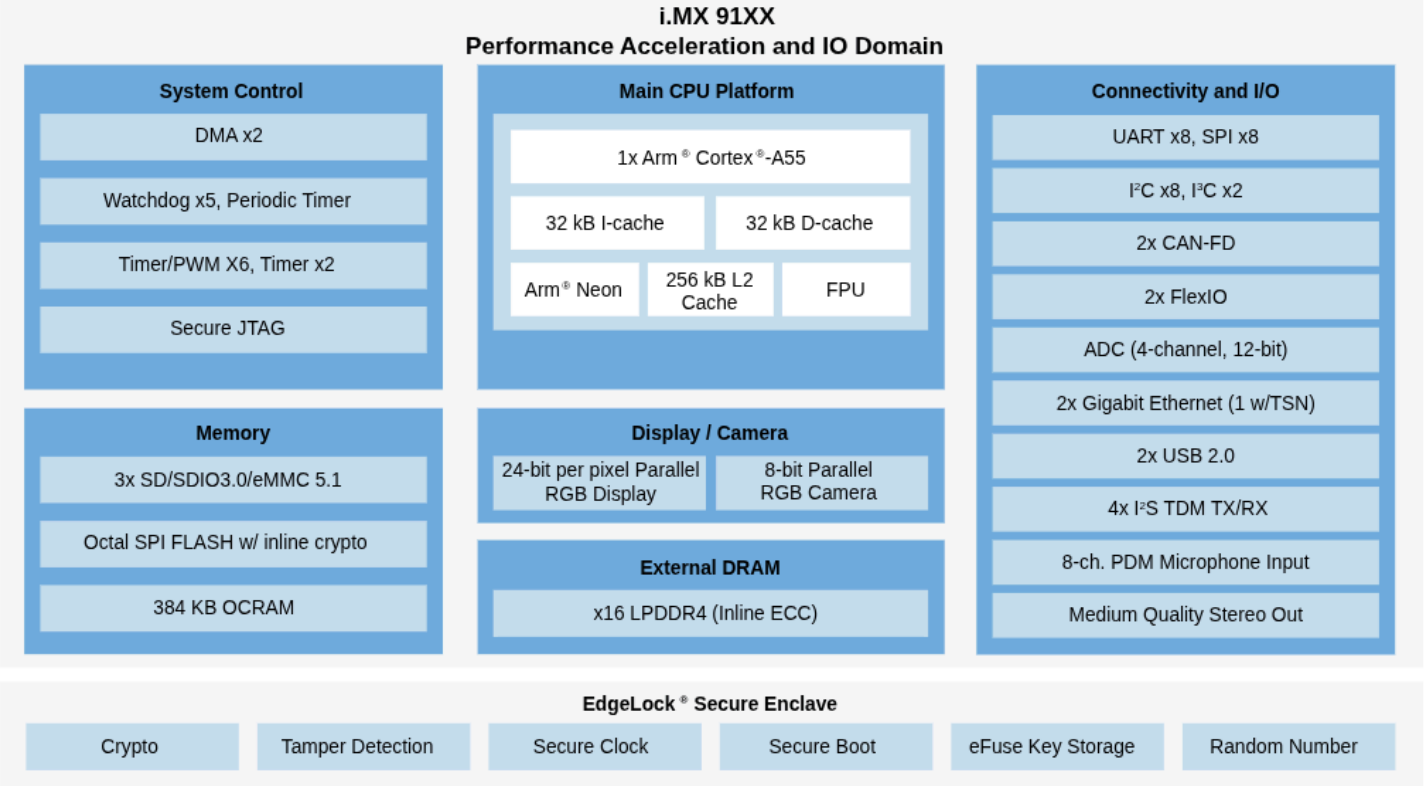
2.3. Block diagram of IMX9x

The i.MX9 family focuses on vision systems, advanced multimedia and industrial automation with high reliability. The i.MX9 is a powerful up to dual Arm® Cortex®-A55 processor with speed up to 1.7 GHz integrated with a microNPU that greatly accelerates machine learning inference. The vision engine is composed of two camera inputs.

Key features of IMX9x

- single or dual Arm® Cortex®-A55 core, up to 1.7 GHz
- Arm® Cortex®-M33 250 MHz processor
- Arm® Ethos™ micro Neural Processing Unit (NPU)
- 1080p60 MIPI CSI (2-lane) camera interface
- 1080p60 MIPI DSI (4-lane), 720p60 LVDS (4-lane), 24-bit parallel RGB Display support
- Arm® TrustZone® and EdgeLock® secure enclave




i.MX 91XX
Performance Acceleration and IO Domain
System Control
DMA x2
Watchdog x5, Periodic Timer
Timer/PWM X6, Timer x2
Secure JTAG
Main CPU Platform
1x Arm® Cortex®-A55
32 kB I-cache
32 kB D-cache
Arm® Neon
256 kB L2 Cache
FPU
Connectivity and I/O
UART x8, SPI x8
I²C x8, I³C x2
2x CAN-FD
2x FlexIO
ADC (4-channel, 12-bit)
2x Gigabit Ethernet (1 w/TSN)
2x USB 2.0
4x I²S TDM TX/RX
8-ch. PDM Microphone Input
Medium Quality Stereo Out
Memory
3x SD/SDIO3.0/eMMC 5.1
Octal SPI FLASH w/ inline crypto
384 KB OCRAM
Display / Camera
24-bit per pixel Parallel RGB Display
8-bit Parallel RGB Camera
External DRAM
x16 LPDDR4 (Inline ECC)
EdgeLock® Secure Enclave
Crypto
Tamper Detection
Secure Clock
Secure Boot
eFuse Key Storage
Random Number

2.4. Additional Information

The i.MX 9x family offers a wide range of options. To facilitate the decision guidance, the selection guide has been extended:

Feature	i.MX93	i.MX91
Cortex®-A55	Up to Dual	Single
Cortex®-M33	Single	No
NPU	Yes	No
GPU	2D	No
Display	1080p60 MIPI DSI 4-lane 720p60 LVDS 4-lane, 24bit parallel RGB	24bit parallel RGB

Family	Subfamily		Cores		Temperature		Frequency	
MIMX93	5	with NPU	2	Dual Core	CVVX	Industrial	MAB	1700 MHz
	3	without NPU	1	Single Core	DVVX	Commercial		
	0	Reduced Performance					DAB	900 MHz
MIMX91	3	Full Feature	1	Single Core	CVVX	Industrial	JAA	1400 MHz
	2	Reduced Performance			DVVX	Commercial	CAA	800 MHZ

For further information regarding the IMX9x CPU, please visit the homepage of NXP: NXP i.MX 9

2.5. Decision guidance byteENGINE IMX9x

The following five steps help identifying the suitable byteENGINE for the specific customer application.

> Step 1: Select the needed CPU

> **Choose Options as described in Additional Information**

> Step 2: Select the needed flash memory capacity

> **Choose eMMC 8 / 16 / 32 / 64 / 128 GB**

> Step 3: Select the needed RAM capacity

> **Choose 512 / 1024 / 1536 / 2048 MB**

> Step 4: Select the needed Pinout configuration

> **Choose OSM-ext or LCD (Details see Pinout functions)**

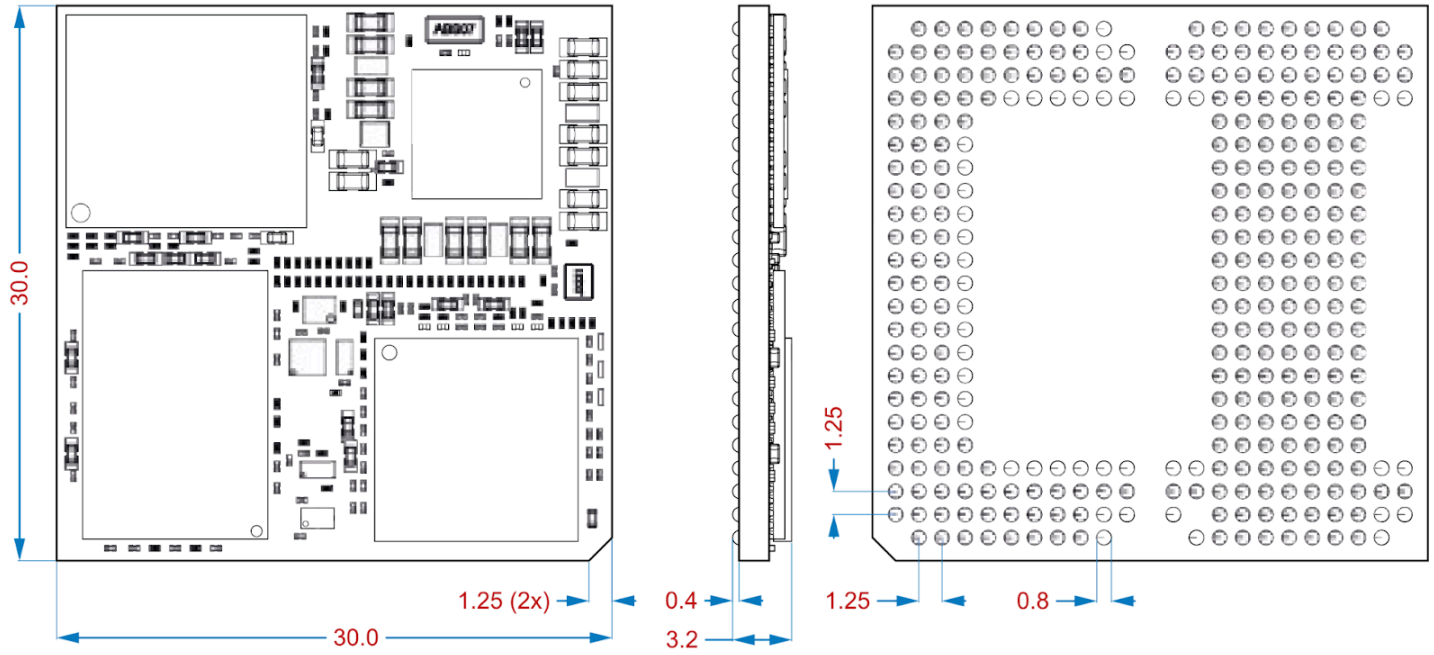
> Step 5: Select the needed temperature range

> **Choose consumer or industrial**

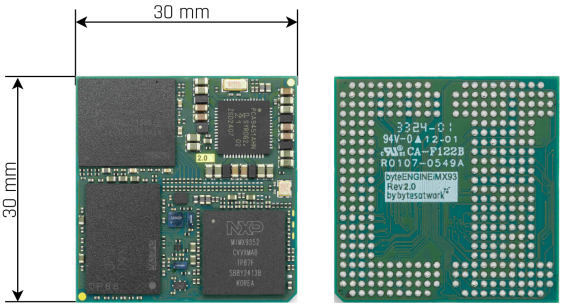
2.6. Dimensions of byteENGINE IMX9x

The following illustration shows all important dimensions for mounting and installation of the industrial computing module byteENGINE IMX9x.

> All dimensions are indicated in millimetres (mm)

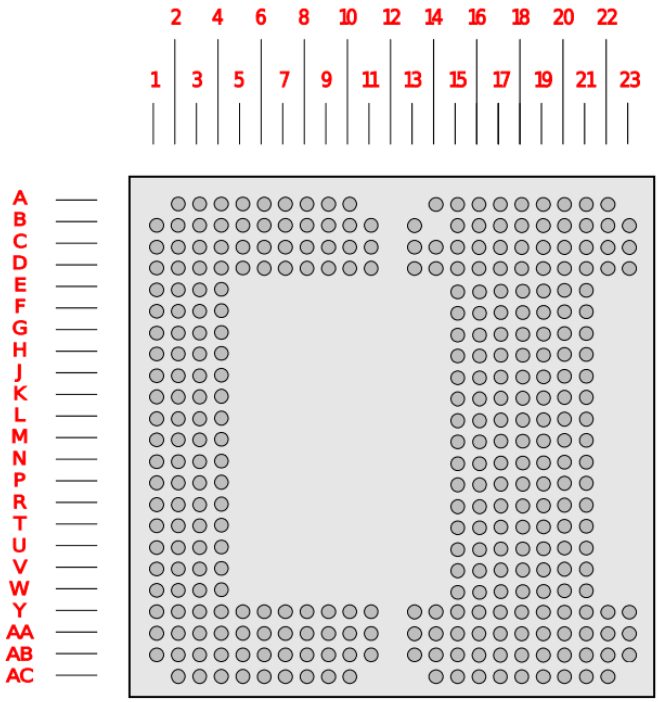


> Module design in scale 1:1:



2.7. byteENGINE IMX9x OSM-S interface

The byteENGINE IMX9x is soldered to the carrier board with 332 contacts. The following picture shows the location of the solder balls on the bottom side of the SOM byteENGINE IMX9x.



https://sget.org

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2.8. Configuration tool for i.MX processors

The **Config Tools for i.MX** is a suite of evaluation and configuration tools that help users from initial evaluation to production software development. Config Tools for i.MX is an easy-to-use way to configure the pins and DDR of the i.MX processor devices.

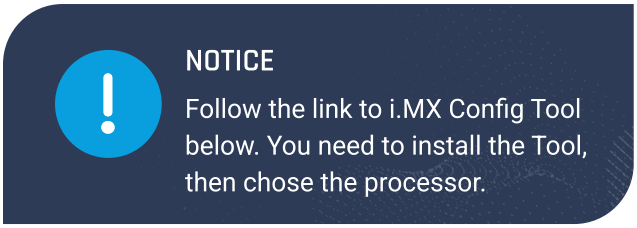
The Config Tools for i.MX is installed as a desktop tool which then loads additional device information through a network connection, but does otherwise not need internet connection. It does not require a project setup, as all the settings are stored in text and generated source files, which then can be easily stored in a version control system or exchanged with other users.

The Pins Tool makes pin configuration easier and faster with an intuitive and easy user interface, which then generates normal C code that can then be used in any C and C++ application. The Pins Tool configures pin signals from multiplexing (muxing) to the electrical properties of pins, and it also creates Device Tree Snippets Include (.dtsi) files and reports in CSV format.

The DDR tool provides two main functionalities: configuration and validation

The DDR configuration provides a user-friendly graphical interface to configure the DDR controller and the DDR PHY. It can be used for tweaking some of the configuration parameters when you want to use different memory modules than the ones received with the board or when you want to optimize the configuration. DDR validation provides different scenarios to verify the DDR performance, by downloading a test image to the processor's internal RAM through a USB connection. The result is sent to the DDR tool via the UART. DDR validation can help verify DDR stability on the board in a non-OS environment.

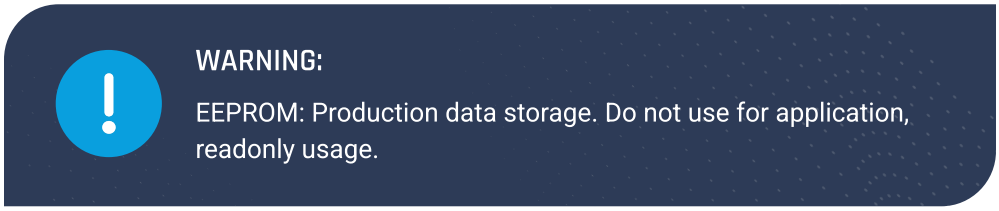
i.MX Config Tool



3. Pinout functions

3.1. Restrictions

These peripherals are internally connected and should not be utilized in the customer design if the components are populated and in use.



Restricted peripherals

I2C2	EEPROM Addr 0x50 - 0x57 PMIC Addr 0x25 IOEXPANDER Addr 0x34
SD4	eMMC

Ball	Pin Name	Used for
Y11	SD1_CLK	eMMC
Y12	SD1_STROBE	eMMC
Y13	SD1_DATA4	eMMC
Y14	SD1_DATA5	eMMC
Y15	SD1_DATA6	eMMC
Y16	SD1_DATA7	eMMC
AA12	SD1_CMD	eMMC
AA13	SD1_DATA3	eMMC
AA14	SD1_DATA0	eMMC
AA15	SD1_DATA1	eMMC
AA16	SD1_DATA2	eMMC

For **Ethernet** the pinout of the OSM Standard and i.MX9x are not compatible. The standard Mode for Ethernet is RGMII, to connect a gigabit ethernet PHY.

RMII is also supported. The iMX9x outputs the RMII_REF_CLK on ENET(X)_TD2. The OSM Standard expects the RMII_REF_ CLK on ETH_X_RMII_TX_CLK pin. To support the RMII Interface an analog switch is placed between ENET(X)_TD2 and ENET(X)_TXC

The analog switch is controlled via ENET_(X)_SDP Pins (N16 / M2). Normally the switch is open, a pulldown is selecting RGMII as default interface mode. To select RMII, ENET_(X)_SDP must be set to 1.8V to close the analog switch

3.2. Module population variants

The OSM Standard defines a general I/O voltage levels of 1.8V. There is an exception for the LCD Interface, which resides on 3.3V. As the iMX9x only supports one power domain for the GPIO Bank, the byteENGINE IMX9x is designed for population variants.

LCD Variant

Supporting 16-bit LCD Panel on 3.3V level

OSM-ext. Variant

Supporting additional peripherals on 1.8V level and LVDS on the RGB Pins as extension to the OSM Standard.

Common Peripherals (1.8V)	
UART1 (2Pin), UART2 (2Pin)	
I2C1 / I2C2	
CAN1 / CAN2	
SAI1 with MCLK	
FLEXSPI1 (QSPI with 1CS)	
RGMII1 / RGMII2	
SD2 (SDCARD with CD)	
USB1 / USB2 (OTG with ID and Enable)	
CSI / DSI	
PWM0 / PWM1 / PWM2	
18 GPIOs on I2Cexpander (I2C2)	
OSM-ext (1.8V)	**LCD (3.3V)**
6 native GPIOs (incl. additional SPI CS)	16 Bit RGB
UART3 (RTC/CTS)	HSYNC, VSYNC, DE, CLK, RST, DISP
UART5 (RTS/CTS)	
UART8 (2Pin)	
SPI7 (1CS)	
LVDS (on RGB Pins, not OSM-S)	
SD3 (4 Bit SDIO)	
PWM3	

3.3. PIN List OSM-ext

Pin List OSM-ext

OSM Pin	MPU Pin	OSM Pin Name	GPIOx / Dedicated Function	Alternative Modes on Pin							Details
				1	2	3	4	5	6	7	
A2	A10	CSI_A_DATA1_N	MIPI_CSI1_D1_N								
A3	B10	CSI_A_DATA1_P	MIPI_CSI1_D1_P								
A4	-	GND	GND								
A5	N/A	CSI_A_DATA2_N									
A6	N/A	CSI_A_DATA2_P									
A7	-	GND	GND								
A8	N/A	USB_C_SSTX_P									
A9	N/A	USB_C_SSTX_N									
A10	-	GND	GND								
A14	P21	UART_A_RX	GPIO2_IO15	FLEXIO1_IO15	LPUART3_RX	LPUART8_RTS_B	LPUART4_RX	LPSPI8_SCK	MMX_C_DATA7	MMX_D_DATA11	
A15	N/A	CH1_RX_N									
A16	N/A	CH1_LINK									
A17	N/A	CH1_TX_N									
A18	N/A	CH0_SYNC_TRIG									
A19	N/A	CH0_RX_N									
A20	N/A	CH0_LINK									
A21	N/A	CH0_TX_N									
A22	F20	UART_C_RX	GPIO1_IO6	LPUART1_CTS_B	LPUART2_RX	LPSPI2_SOUT	TPM1_CH2	SAI1_MCLK			
B1	B11	CSI_A_DATA0_P	MIPI_CSI1_D0_P								

Pin List OSM-ext

OSM Pin	MPU Pin	OSM Pin Name	GPIOx / Dedicated Function	Alternative Modes on Pin							Details
				1	2	3	4	5	6	7	
B2	-	GND	GND								
B3	D10	CSI_A_CLOCK_N	MIPI_CSI1_CLK_N								
B4	E10	CSI_A_CLOCK_P	MIPI_CSI1_CLK_P								
B5	-	GND	GND								
B6	N/A	CSI_A_DATA3_N									
B7	N/A	CSI_A_DATA3_P									
B8	-	GND	GND								
B9	-	GND	GND								
B10	N/A	USB_C_SSRX_P									
B11	N/A	USB_C_SSRX_N									
B13	P20	UART_A_TX	GPIO2_IO14	FLEXIO1_IO14	LPUART3_TX	LPUART8_CTS_B	LPUART4_TX	LPSPI8_SOUT	MMX_C_DATA6	MMX_D_DATA10	
B15	N/A	CH1_RX_P									
B16	N/A	CH1_ACT									
B17	N/A	CH1_TX_P									
B18	N/A	CH1_SYNC_TRIG									
B19	N/A	CH0_RX_P									
B20	N/A	CH0_ACT									
B21	N/A	CH0_TX_P									
B22	N/A	Vendor Defined									
B23	F21	UART_C_TX	GPIO1_IO7	LPUART2_TX	LPUART1_RTS_B	LPSPI2_SCK	TPM1_CH3				
C1	A11	CSI_A_DATA0_N	MIPI_CSI1_D0_N								
C2	Y3	CAM_MCK	GPIO3_IO27	FLEXIO1_IO27	CCM_CLKO2						

Pin List OSM-ext

OSM Pin	MPU Pin	OSM Pin Name	GPIOx / Dedicated Function	Alternative Modes on Pin							Details
				1	2	3	4	5	6	7	
C3	N/A	CAM_A_SDA/ CSI_A_TX_N									
C4	N/A	CAM_A_SCL/ CSI_A_TX_P									
C5	-	VCC_6_TEST	VDD_3V3								
C6	Y7	ETH_B_MDC	GPIO4_IO14	FLEXIO2_IO14	LPUART4_DCB_B	SAI2_RX_SYNC	ENET1_MDC (FEC)				
C7	AA6	ETH_B_MDIO	GPIO4_IO15	FLEXIO2_IO15	LPUART4_RIN_B	SAI2_RX_BCLK	ENET1_MDIO (FEC)				
C8	N/A	USB_C_OC#									
C9	N/A	USB_C_VBUS									
C10	N/A	USB_C_EN									
C11	-	GND	GND								
C13	R20	UART_A_RTS	GPIO2_IO17	FLEXIO1_IO17	LPUART3_RTS_B	LPUART4_RTS_B	LPSPI4_PCS1	SAI3_MCLK	MMX_C_DATA8	MMX_D_DATA13	
C14	R21	UART_A_CTS	GPIO2_IO16	FLEXIO1_IO16	LPUART3_CTS_B	LPUART4_CTS_B	LPSPI4_PCS2	SAI3_TX_BCLK	PDM_BS02	MMX_D_DATA12	
C15	N/A	CH1_RXC									
C16	N/A	Vendor Defined									
C17	N/A	CH1_TXC									
C18	N/A	TEST_GENERIC									
C19	N/A	CH0_RXC									
C20	R16	SDIO_A_IOPWR	NVCC_SD2								
C21	N/A	CH0_TXC									
C22	N21	UART_D_RX	GPIO2_IO13	FLEXIO1_IO13	LPUART8_RX	LPSPI8_SIN	TPM4_CH2	LPI2C8_SCL	PDM_BS03	MMX_D_DATA09	
C23	N20	UART_D_TX	GPIO2_IO12	SAI3_RX_SYNC	LPUART8_TX	LPSPI8_PCS0	TPM3_CH2	LPI2C8_SDA	PDM_BS02	MMX_D_DATA08	
D1	-	GND	GND								
D2	N/A	ETH_B_(R)(G)MII_ CRS									

Pin List OSM-ext

OSM Pin	MPU Pin	OSM Pin Name	GPIOx / Dedicated Function	Alternative Modes on Pin							Details
				1	2	3	4	5	6	7	
D3	-	GPIO_C_0	I2C2_EXP_IO14								
D4	-	GPIO_C_1	I2C2_EXP_IO15								
D5	-	GND	GND								
D6	G21	Vendor Defined	BOOT_MODE[2]	GPIO1_IO11	LPUART2_DTR_B	LPSPI1_PCS0	SAI1_TX_SYNC	SAI1_TX_DATA01	MQS1_LEFT		
D7	H21	Vendor Defined	BOOT_MODE[3]	GPIO1_IO13	LPUART2_RTS_B	LPUART1_DTR_B	LPSPI1_SCK	SAI1_TX_DATA00	CAN1_TX		
D8	-	GND	GND								
D9	N/A	USB_C_ID									
D10	N/A	USB_C_D_P									
D11	N/A	USB_C_D_N									
D13	J21	UART_B_TX	GPIO2_IO00	FLEXIO1_IO00	LPUART5_TX	LPSPI6_PCS0	LPI2C3_SDA	LPI2C5_SDA	MMX_C_CLK	MMX_D_CLK	
D14	J20	UART_B_RX	GPIO2_IO01	FLEXIO1_IO01	LPUART5_RX	LPSPI6_SIN	LPI2C3_SCL	LPI2C5_SCL	MMX_C_DATA00	MMX_D_DE	
D15	K21	UART_B_RTS	GPIO2_IO03	FLEXIO1_IO03	LPUART5_RTS_B	LPSPI6_SCK	LPI2C4_SCL	LPI2C6_SCL	MMX_C_HSYNC	MMX_D_HSYNC	
D16	K20	UART_B_CTS	GPIO2_IO02	FLEXIO1_IO02	LPUART5_CTS_B	LPSPI6_SOUT	LPI2C4_SDA	LPI2C6_SDA	MMX_C_VSYNC	MMX_D_VSYNC	
D17	-	GPIO_A_0	I2C2_EXP_IO00								
D18	-	GND	GND								
D19	-	GPIO_B_0	I2C2_EXP_IO06								
D20	N/A	SDIO_A_WP									
D21	-	SDIO_A_PWR_EN	VSD_3V3								
D22	E20	UART_CON_RX	GPIO1_IO04	LPUART1_RX	LPSPI2_SIN	TPM1_CH0	S400_UART_RX				
D23	E21	UART_CON_TX	GPIO1_IO05	LPUART1_TX	LPSPI2_PCS0	TPM1_CH1	S400_UART_TX				
E1	N/A	ETH_B_(R)(G)MII_COL									
E2	-	GND	GND								

Pin List OSM-ext

OSM Pin	MPU Pin	OSM Pin Name	GPIOx / Dedicated Function	Alternative Modes on Pin							Details
				1	2	3	4	5	6	7	
E3	-	GPIO_C_2/ CAM_B_PWR	I2C2_EXP_IO16								
E4	-	GPIO_C_3/ CAM_B_RST#	I2C2_EXP_IO17								
E15	-	GND	GND								
E16	N/A	ETH_A_(R)(G)MII_ CRS									
E17	-	GPIO_A_1	I2C2_EXP_IO01								
E18	AA2	PWM_0	GPIO3_IO26	FLEXIO1_IO26	CCM_CLKO1						
E19	-	GPIO_B_1	I2C2_EXP_IO07								
E20	Y19	SDIO_A_CMD	GPIO3_IO02	FLEXIO1_IO02	USDHC2_CMD	ENET1_EVENT0 _IN (FEC)	CCM_OBSERVE1	I3C2_PUR	I3C2_PUR_B		
E21	-	GND	GND								
F1	U8	ETH_B_(S)(R)(G) MII_TXD1	GPIO4_IO18	FLEXIO2_IO18	LPUART4_RTS_B	SAI2_RX_DATA02	ENET1_RGMII_TD1 (FEC)				
F2	T10	ETH_B_(S)(R)(G) MII_TXD3	GPIO4_IO16	FLEXIO2_IO16	SAI2_RX_DATA00	ENET1_RGMII_TD3 (FEC)					
F3	N17	GPIO_C_4	GPIO2_IO10	FLEXIO1_IO10	LPUART7_CTS_B	LPSPI3_SOUT	TPM4_EXTCLK	MMX_C_DATA04	MMX_D_DATA06	LPI2C8_SDA	
F4	T21	GPIO_C_5	GPIO2_IO21	LPSPI4_SCK	LPSPI5_SCK	TPM4_CH1	SAI3_RX_BCLK	SAI3_TX_DATA00	PDM_CLK	MMX_D_DATA17	
F15	N/A	ETH_A_(R)(G)MII_ COL									
F16	-	GND	GND								
F17	-	GPIO_A_2	I2C2_EXP_IO02								
F18	R17	PWM_1	GPIO2_IO19	LPSPI5_SIN	LPSPI4_SIN	TPM6_CH2	MMX_D_DATA15	SAI3_RX_SYNC	SAI3_TX_DATA00	PDM_BS03	LEVEL SHIFTER
F19	-	GPIO_B_2	I2C2_EXP_IO8								
F20	-	GND	GND								
F21	AA19	SDIO_A_CLK	GPIO3_IO01	FLEXIO1_IO01	USDHC2_CLK	ENET_QOS_EVENT 0_OUT	CCM_OBSERVE0	I3C2_SDA			

Pin List OSM-ext

OSM Pin	MPU Pin	OSM Pin Name	GPIOx / Dedicated Function	Alternative Modes on Pin							Details
				1	2	3	4	5	6	7	
G1	T8	ETH_B_(S)(R)(G)MII_TXD0	GPIO4_IO19	FLEXIO2_IO19	LPUART4_TX	SAI2_RX_DATA03	ENET1_RGMII_TD0 (FEC)				
G2	V8	ETH_B_(S)(R)(G)MII_TXD2	GPIO4_IO17	FLEXIO2_IO17	SAI2_RX_DATA01	ENET1_RGMII_TD2 (FEC)	ENET1_TX_CLK (FEC)				
G3	T20	GPIO_C_6/ CAM_A_PWR	GPIO2_IO20	FLEXIO1_IO20	LPSPI5_SOUT	LPSPI4_SOUT	TPM3_CH1	MMX_D_DATA16	SAI3_RX_DATA00	PDM_BS00	
G4	W20	GPIO_C_7/ CAM_A_RST#	GPIO2_IO28	FLEXIO1_IO28	LPI2C3_SDA						
G15	T12	ETH_A_(S)(R)(G)MII_TXD1	GPIO4_IO04	FLEXIO2_IO04	LPUART3_RTS_B	ENET_QOS_RGMII_TD1	I3C2_PUR	I3C2_PUR_B	USB1_OTG_OC		
G16	V12	ETH_A_(S)(R)(G)MII_TXD3	GPIO4_IO02	FLEXIO2_IO02	CAN2_TX	ENET_QOS_RGMII_TD3	USB2_OTG_ID				
G17	-	GPIO_A_3	I2C2_EXP_IO03								
G18	V4	PWM_2	GPIO4_IO29	FLEXIO2_IO29	CCM_CLKO4						
G19	-	GPIO_B_3	I2C2_EXP_IO09								
G20	Y18	SDIO_A_D0	GPIO3_IO03	FLEXIO1_IO03	USDHC2_DATA0	ENET1_EVENT0_OUT (FEC)	CAN2_TX	CCM_OBSERVE2			
G21	AA18	SDIO_A_D1	GPIO3_IO04	FLEXIO1_IO04	USDHC2_DATA1	ENET1_EVENT1_IN (FEC)	CAN2_RX				
H1	U6	ETH_B_(R)(G)MII_TX_CLK	GPIO4_IO21	FLEXIO2_IO21	SAI2_TX_BCLK	ENET1_RGMII_TXC (FEC)	ENET1_TX_ER (FEC)				
H2	-	GND	GND								
H3	N/A	RGB_CS#									
H4	-	GND	GND								
H15	W11	ETH_A_(S)(R)(G)MII_TXD0	GPIO4_IO05	FLEXIO2_IO05	LPUART3_TX	ENET_QOS_RGMII_TD0					
H16	U12	ETH_A_(S)(R)(G)MII_TXD2	GPIO4_IO03	FLEXIO2_IO03	ENET_QOS_RGMII_TD2	ENET_QOS_REF_CLK	CAN2_RX	USB2_OTG_OC			
H17	-	GPIO_A_4	I2C2_EXP_IO04								
H18	Y21	PWM_3	GPIO2_IO29	FLEXIO1_IO29	LPI2C3_SCL						

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OSM Pin	MPU Pin	OSM Pin Name	GPIOx / Dedicated Function	Alternative Modes on Pin							Details
				1	2	3	4	5	6	7	
H19	-	GPIO_B_4	I2C2_EXP_IO10								
H20	Y20	SDIO_A_D2	GPIO3_IO05	FLEXIO1_IO05	USDHC2_DATA2	ENET1_EVENT1_OUT (FEC)	MQS2_RIGHT				
H21	AA20	SDIO_A_D3	GPIO3_IO06	FLEXIO1_IO06	USDHC2_DATA3	MQS2_LEFT	LPTMR2_ALT1				
J1	AA4	ETH_B_(S)(R)(G)MII_RXD0	GPIO4_IO24	FLEXIO2_IO24	LPUART4_RX	SAI2_TX_DATA02	ENET1_RGMII_RD0 (FEC)				
J2	V6	ETH_B_(R)(G)MII_TX_EN(_ER)	GPIO4_IO20	FLEXIO2_IO20	LPUART4_DTR_B	SAI2_TX_SYNC	ENET1_RGMII_TX_CTL (FEC)				
J3	N/A	RGB_RESET#									
J4	N/A	RGB_DE									
J15	U10	ETH_A_(R)(G)MII_TX_CLK	GPIO4_IO07	FLEXIO2_IO07	ENET_QOS_TX_CLK	ENET_QOS_TX_ER					
J16	-	GND	GND								
J17	-	GPIO_A_5	I2C2_EXP_IO05								
J18	N/A	PWM_4									
J19	-	GPIO_B_5	I2C2_EXP_IO11								
J20	-	GND	GND								
J21	Y17	SDIO_A_CD#	GPIO3_IO00	FLEXIO1_IO00	USDHC2_CD_B	ENET_QOS_EVENT0_IN	I3C2_SCL				
K1	Y5	ETH_B_(S)(R)(G)MII_RXD1	GPIO4_IO25	FLEXIO2_IO25	SAI2_TX_DATA03	ENET1_RGMII_RD1 (FEC)	SPDIF_IN				
K2	N/A	ETH_B_(R)(G)MII_RX_ER									
K3	N/A	RGB_HSYNC									
K4	N/A	RGB_DISP									
K15	AA8	ETH_A_(S)(R)(G)MII_RXD0	GPIO4_IO10	FLEXIO2_IO10	LPUART3_RX	ENET_QOS_RGMII_RD0					
K16	V10	ETH_A_(R)(G)MII_TX_EN(_ER)	GPIO4_IO06	FLEXIO2_IO06	LPUART3_DTR_B	ENET_QOS_RGMII_TX_CTL					

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OSM Pin	MPU Pin	OSM Pin Name	GPIOx / Dedicated Function	Alternative Modes on Pin							Details
				1	2	3	4	5	6	7	
K17	M20	GPIO_A_6	GPIO2_IO08	FLEXIO1_IO08	LPUART7_TX	LPSPI3_PCS0	TPM6_CH0	MMX_C_DATA02	MMX_D_DATA04	LPI2C7_SDA	
K18	N/A	PWM_5									
K19	-	GPIO_B_6	I2C2_EXP_IO12								
K20	U18	SDIO_B_CLK	GPIO2_IO22	FLEXIO1_IO22	USDHC3_CLK	TPM5_CH1	TPM6_EXTCLK	LPI2C5_SDA	SPDIF_IN	MMX_D_DATA18	
K21	U20	SDIO_B_CMD	GPIO2_IO23	FLEXIO1_IO23	USDHC3_CMD	TPM6_CH1	LPI2C5_SCL	SPDIF_OUT	MMX_D_DATA19		
L1	Y4	ETH_B_(R)(G)MII_RX_DV(_ER)	GPIO4_IO22	FLEXIO2_IO22	LPUART4_DSR_B	SAI2_TX_DATA00	ENET1_RGMII_RX_CTL (FEC)				
L2	-	GND	GND								
L3	N/A	RGB_VSYNC									
L4	-	GND	GND								
L15	Y9	ETH_A_(S)(R)(G)MII_RXD1	GPIO4_IO11	FLEXIO2_IO11	LPUART3_CTS_B	ENET_QOS_RGMII_RD1	LPTMR2_ALT1				
L16	N/A	ETH_A_(R)(G)MII_RX_ER									
L17	M21	GPIO_A_7	GPIO2_IO09	FLEXIO1_IO09	LPUART6_RTS_B	LPSPI3_SIN	TPM3_EXTCLK	MMX_C_DATA03	MMX_D_DATA05	LPI2C7_SCL	
L18	-	GND	GND								
L19	-	GPIO_B_7	I2C2_EXP_IO13								
L20	U21	SDIO_B_D0	GPIO2_IO24	FLEXIO1_IO24	LPSPI6_PCS1	USDHC3_DATA0	TPM3_CH3	MMX_D_DATA20	JTAG_MUX_TDO		
L21	V21	SDIO_B_D1	GPIO2_IO25	FLEXIO1_IO25	LPSPI7_PCS1	USDHC3_DATA1	TPM4_CH3	MMX_D_DATA21	CAN2_TX	JTAG_MUX_TCK	
M1	AA5	ETH_B_(R)(G)MII_RXD2	GPIO4_IO26	FLEXIO2_IO26	LPUART4_CTS_B	SAI2_MCLK	ENET1_RGMII_RD2	MQS2_RIGHT			
M2	N/A	ETH_B_SDP	0 = RGMII, 1=RMII (TXCLK and TD2 are connected internally)								
M3	N/A	RGB_B5									
M4	N/A	RGB_(PIXEL)CLK									

Pin List OSM-ext

OSM Pin	MPU Pin	OSM Pin Name	GPIOx / Dedicated Function	Alternative Modes on Pin							Details
				1	2	3	4	5	6	7	
M15	Y8	ETH_A_(R)(G)MII_RX_DV(_ER)	GPIO4_IO08	FLEXIO2_IO08	LPUART3_DSR_B	ENET_QOS_RGMII_RX_CTL	USB_OTG_PWR2				
M16	-	GND	GND								
M17	-	ETH_IOPWR	VDD_1V8								
M18	B19	ADC_0	ADC_IN0								
M19	-	VCC_2_TEST2	VDD_SOC_0V85								
M20	-	GND	GND								
M21	V20	SDIO_B_D2	GPIO2_IO26	LPSPI8_PCS1	USDHC3_DATA2	TPM5_CH3	MMX_D_DATA22	SAI3_TX_SYNC	PDM_BS01	JTAG_MUX_TDI	
N1	Y6	ETH_B_(R)(G)MII_RXD3	GPIO4_IO27	FLEXIO2_IO27	ENET1_RGMII_RD3	MQS2_LEFT	SPDIF_OUT	SPDIF_IN			
N2	N/A	RESERVED									
N3	N/A	RGB_B3									
N4	N/A	RGB_B4									
N15	AA9	ETH_A_(R)(G)MII_RXD2	GPIO4_IO12	FLEXIO2_IO12	ENET_QOS_RGMII_RD2						
N16	N/A	ETH_A_SDP	0 = RGMII, 1=RMII (TXCLK and TD2 are connected internally)								PULLDOWN_10K
N17	Y1	JTAG_TCK(SWCLK)	GPIO3_IO30	FLEXIO1_IO30	LPUART5_CTS_B	JTAG_MUX_TCK					
N18	A20	ADC_1	ADC_IN1								
N19	W2	JTAG_TMS(SWDIO)	GPIO3_IO29	FLEXIO2_IO31	LPUART5_RTS_B	JTAG_MUX_TMS					
N20	W21	SDIO_B_D3	GPIO2_IO27	FLEXIO1_IO27	LPSPI5_PCS1	USDHC3_DATA3	TPM6_CH3	MMX_D_DATA23	CAN2_RX	JTAG_MUX_TMS	
N21	N/A	SDIO_B_D4									
P1	AA3	ETH_B_(R)(G)MII_RX_CLK	GPIO4_IO23	FLEXIO2_IO23	SAI2_TX_DATA01	ENET1_RGMII_RXC (FEC)	ENET1_RX_ER (FEC)				
P2	-	GND	GND								

Pin List OSM-ext

OSM Pin	MPU Pin	OSM Pin Name	GPIOx / Dedicated Function	Alternative Modes on Pin							Details
				1	2	3	4	5	6	7	
P3	B1	RGB_B2	LVDS_D3_N								
P4	-	GND	GND								
P15	Y10	ETH_A_(R)(G)MII_RXD3	GPIO4_IO13	FLEXIO2_IO13	ENET_QOS_RGMII_RD3	LPTMR2_ALT3					
P16	N/A	Vendor Defined									
P17	W1	JTAG_TDI	GPIO3_IO28	FLEXIO2_IO30	LPUART5_RX	CAN2_TX	MQS2_LEFT	JTAG_MUX_TDI			
P18	-	GND	GND								
P19	N/A	JTAG_RTCK									
P20	N/A	SDIO_B_D5									
P21	N/A	SDIO_B_D6									
R1	-	GND	GND								
R2	N/A	PCIe_SM_ALERT#									
R3	N/A	RGB_B1									
R4	C1	RGB_B0	LVDS_D3_P								
R15	AA7	ETH_A_(R)(G)MII_RX_CLK	GPIO4_IO09	FLEXIO2_IO09	ENET_QOS_RX_CLK	ENET_QOS_RX_ER					
R16	-	GND	GND								
R17	Y2	JTAG_TDO(SWO)	GPIO3_IO31	FLEXIO1_IO31	LPUART5_TX	CAN2_RX	MQS2_RIGHT	JTAG_MUX_TDO			
R18	F21	BOOT_SEL1#	BOOT_MODE[1]								ONLY FOR FIRST <1ms
R19	N/A	JTAG_nTRST									
R20	-	GND	GND								
R21	N/A	SDIO_B_D7									
T1	N/A	PCIe_SMCLK									
T2	N/A	PCIe_WAKE#									

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OSM Pin	MPU Pin	OSM Pin Name	GPIOx / Dedicated Function	Alternative Modes on Pin							Details
				1	2	3	4	5	6	7	
T3	N/A	RGB_G4									
T4	A2	RGB_G5	LVDS_D2_N								
T15	AA10	ETH_MDIO	GPIO4_IO01	FLEXIO2_IO01	LPUART3_RIN_B	ENET_QOS_MDIO	I3C2_SDA	USB_OTG_PWR1			
T16	AA11	ETH_MDC	GPIO4_IO00	FLEXIO2_IO00	LPUART3_DCB_B	ENET_QOS_MDC	I3C2_SCL	USB_OTG_ID1			
T17	N/A	FORCE_RECOVERY#									
T18	N/A	I2S_B_LRCLK									
T19	N/A	I2S_B_BITCLK									
T20	-	SDIO_B_IOPWR	VDD_1V8								
T21	N/A	SDIO_B_CD#									
U1	N/A	PCIe_SMDAT									
U2	-	GND	GND								
U3	B2	RGB_G3	LVDS_D2_P								
U4	-	GND	GND								
U15	V14	SPI_A_SDI_(IO1)	GPIO3_IO23	FLEXIO1_IO23	USDHC3_DATA1	FLEXSPI1_A_DATA01					
U16	V16	SPI_A_SCK	GPIO3_IO20	FLEXIO1_IO20	USDHC3_CLK	FLEXSPI1_A_SCLK					
U17	N/A	RESET_IN#	PMIC_RST_B								PULLUP_100K_NVCC_BBSM_1V8
U18	-	VCC_OUT_IO	NVCC_GPIO								
U19	E21	BOOT_SEL0#	BOOT_MODE[0]								ONLY FOR FIRST <1ms
U20	N/A	SDIO_B_WP									
U21	N/A	SDIO_B_PWR_EN									
V1	-	GND	GND								

Pin List OSM-ext

OSM Pin	MPU Pin	OSM Pin Name	GPIOx / Dedicated Function	Alternative Modes on Pin							Details
				1	2	3	4	5	6	7	
V2	N/A	PCIe_A_PERST#									
V3	A4	RGB_G1	LVDS_D1_N								
V4	N/A	RGB_G2									
V15	T16	SPI_A_SDO_(IO0)	GPIO3_IO22	FLEXIO1_IO22	USDHC3_DATA0	FLEXSPI1_A_DATA00					
V16	-	GND	GND								
V17	-	CARRIER_PWR_EN	VDD_1V8								PULLDOWN_10k
V18	U4	I2S_MCLK	GPIO4_IO28	FLEXIO2_IO28	CCM_CLKO3						
V19	N/A	I2S_B_DATA_IN									
V20	-	GND	GND								
V21	H20	I2S_A_DATA_IN	GPIO1_IO14	LPUART2_DSR_B	LPSPI1_SOUT	SAI1_RX_DATA00	SAI1_MCLK	MQS1_RIGHT			
W1	N/A	PCIe_REFCLK_P									
W2	N/A	PCIe_CLKREQ#									
W3	-	GND	GND								
W4	B4	RGB_G0	LVDS_D1_P								
W15	T14	SPI_A_HOLD_(IO3)	GPIO3_IO25	FLEXIO1_IO25	USDHC3_DATA3	FLEXSPI1_A_DATA03					
W16	U14	SPI_A_WP_(IO2)	GPIO3_IO24	FLEXIO1_IO24	USDHC3_DATA2	FLEXSPI1_A_DATA02					
W17	N/A	RTC_PWR									
W18	G21	I2S_A_LRCLK	GPIO1_IO11	LPUART2_DTR_B	LPSPI1_PCS0	SAI1_TX_SYNC	SAI1_TX_DATA01	MQS1_LEFT			
W19	N/A	I2S_B_DATA_OUT									
W20	G20	I2S_A_BITCLK	GPIO1_IO12	LPUART2_CTS_B	LPUART1_DSR_B	LPSPI1_SIN	SAI1_TX_BCLK	CAN1_RX			
W21	H21	I2S_A_DATA_OUT	GPIO1_IO13	LPUART2_RTS_B	LPUART1_DTR_B	LPSPI1_SCK	SAI1_TX_DATA00	CAN1_TX			
Y1	N/A	PCIe_REFCLK_N									

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OSM Pin	MPU Pin	OSM Pin Name	GPIOx / Dedicated Function	Alternative Modes on Pin							Details
				1	2	3	4	5	6	7	
Y2	-	GND	GND								
Y3	-	VCC_5_TEST	LPD4_VDD2_1V1								
Y4	A5	RGB_R5	LVDS_D0_N								
Y5	N/A	RGB_R4									
Y6	N/A	RGB_R2									
Y7	B3	RGB_R0	LVDS_CLK_P								
Y8	-	VCC_IN_5V	VCC_IN_5V								
Y9	-	VCC_IN_5V	VCC_IN_5V								
Y10	-	VCC_IN_5V	VCC_IN_5V								
Y11	-	VCC_IN_5V	VCC_IN_5V								
Y13	N/A	CARRIER_STBY#									
Y14	N/A	RESET_OUT#									
Y15	U16	SPI_A_CS0#	GPIO3_IO21	FLEXIO1_IO21	USDHC3_CMD	FLEXSPI1_A_SS0_B					
Y16	-	VCC_3_TEST	VCC_1V8								
Y17	-	VCC_IN_5V	VCC_IN_5V								
Y18	-	GND	GND								
Y19	N/A	VCC_IN_3V3									
Y20	-	VCC_4_TEST	VDD_ANA_0V8								
Y21	L21	SPI_B_SCK	GPIO2_IO07	FLEXIO1_IO07	LPUART6_RTS_B	LPSPI3_PCS1	LPSPI7_SCK	MMX_C_DATA01	MMX_D_DATA03	LPI2C7_SCL	
Y22	L18	SPI_B_SDI	GPIO2_IO05	FLEXIO1_IO05	LPUART6_RX	LPSPI7_SIN	TPM4_CH0	MMX_D_DATA01	LPI2C6_SCL	PDM_BS00	
Y23	L20	SPI_B_SDO	GPIO2_IO06	FLEXIO1_IO06	LPUART6_CTS_B	LPSPI7_SOUT	TPM5_CH0	MMX_D_DATA02	LPI2C7_SDA	PDM_BS01	
AA1	-	GND	GND								
AA2	N/A	RESERVED									

Pin List OSM-ext

OSM Pin	MPU Pin	OSM Pin Name	GPIOx / Dedicated Function	Alternative Modes on Pin							Details
				1	2	3	4	5	6	7	
AA3	N/A	DSI_TE									
AA4	-	GND	GND								
AA5	B5	RGB_R3	LVDS_D0_P								
AA6	A3	RGB_R1	LVDS_CLK_N								
AA7	-	GND	GND								
AA8	-	GND	GND								
AA9	A19	PWR_BTN#	ONOFF								PULLUP_100K_NVCC_BBSM_1V8
AA10	-	GND	GND								
AA11	-	GND	GND								
AA13	N/A	RESERVED									
AA14		GND	GND								
AA15	C20	I2C_A_SCL	GPIO1_IO00	LPUART1_DCB_B	TPM2_CH0	LPI2C1_SCL	I3C1_SCL				PULLUP_2K2_VDD_1V8
AA16	C21	I2C_A_SDA	GPIO1_IO01	LPUART1_RIN_B	TPM2_CH1	LPI2C1_SDA	I3C1_SDA				PULLUP_2K2_VDD_1V8
AA17	-	GND	GND								
AA18	N/A	V_BAT									
AA19	-	GND	GND								
AA20	D20	I2C_B_SCL	GPIO1_IO02	LPUART2_DCB_B	TPM2_CH2	SAI1_RX_SYNC	LPI2C2_SCL	I3C1_PUR	I3C1_PUR_B		PULLUP_2K2_VDD_1V8
AA21	D21	I2C_B_SDA	GPIO1_IO03	LPUART2_RIN_B	TPM2_CH3	SAI1_RX_BCLK	LPI2C2_SDA				PULLUP_2K2_VDD_1V8
AA22	-	GND	GND								
AA23	L17	SPI_B_CS0#	GPIO2_IO04	FLEXIO1_IO04	LPUART6_TX	LPSPI7_PCS0	TPM3_CH0	MMX_D_DATA00	LPI2C6_SDA		
AB1	N/A	PCIe_A_HSI0_P									

Pin List OSM-ext

OSM Pin	MPU Pin	OSM Pin Name	GPIOx / Dedicated Function	Alternative Modes on Pin							Details
				1	2	3	4	5	6	7	
AB2	N/A	PCIe_A_HSI0_N									
AB3	-	GND	GND								
AB4	B9	DSI_DATA3_P/ LVDS_A_LANE3_P	MIPI_DSI1_D3_P								
AB5	A9	DSI_DATA3_N/ LVDS_A_LANE3_N	MIPI_DSI1_D3_N								
AB6	-	GND	GND								
AB7	E6	DSI_CLOCK_P/ LVDS_A_CLK_P	MIPI_DSI1_CLK_P								
AB8	D6	DSI_CLOCK_N/ LVDS_A_CLK_N	MIPI_DSI1_CLK_N								
AB9	-	GND	GND								
AB10	B6	DSI_DATA0_P/ LVDS_A_LANE0_P	MIPI_DSI1_D0_P								
AB11	A6	DSI_DATA0_N/ LVDS_A_LANE0_N	MIPI_DSI1_D0_N								
AB13	A14	USB_A_D_N	USB1_D_N								
AB14	C11	USB_A_ID	USB1_ID								
AB15	-	GND	GND								
AB16	F12	USB_A_VBUS	USB1_VBUS								
AB17	J17	CAN_A_RX	GPIO1_IO09	LPSPI1_PCS1	TPM1_EXTCLK	PDM_BS00	CAN1_RX	MQS1_RIGHT	LPTMR1_ALT2		
AB18	N/A	V_BAT									
AB19	Y2	CAN_B_RX	GPIO3_IO31	FLEXIO1_IO31	LPUART5_TX	CAN2_RX	MQS2_RIGHT	JTAG_MUX_TDO			
AB20	E14	USB_B_VBUS	USB2_VBUS								
AB21	-	GND	GND								
AB22	E12	USB_B_ID	USB2_ID								
AB23	A15	USB_B_D_N	USB2_D_N								

Pin List OSM-ext

OSM Pin	MPU Pin	OSM Pin Name	GPIOx / Dedicated Function	Alternative Modes on Pin							Details
				1	2	3	4	5	6	7	
AC2	N/A	PCIe_A_HSO0_P									
AC3	N/A	PCIe_A_HSO0_N									
AC4	-	GND	GND								
AC5	B8	DSI_DATA2_P/ LVDS_A_LANE2_P	MIPI_DSI1_D2_P								
AC6	A8	DSI_DATA2_N/ LVDS_A_LANE2_N	MIPI_DSI1_D2_N								
AC7	-	GND	GND								
AC8	B7	DSI_DATA1_P/ LVDS_A_LANE1_P	MIPI_DSI1_D1_P								
AC9	A7	DSI_DATA1_N/ LVDS_A_LANE1_N	MIPI_DSI1_D1_N								
AC10	-	GND	GND								
AC14	B14	USB_A_D_P	USB1_D_P								
AC15	N/A	USB_A_OC#									
AC16	N18	USB_A_EN	GPIO2_IO11	FLEXIO1_IO11	LPUART7_RTS_B	LPSPI3_SCK	TPM5_EXTCLK	MMX_C_DATA05	MMC_D_DATA07	LPI2C8_SCL	LEVEL SHIFTER
AC17	G17	CAN_A_TX	GPIO1_IO08	PDM_CLK	CAN1_TX	MQS1_LEFT	LPTMR1_ALT1				
AC18	N/A	DEBUG_EN									
AC19	W1	CAN_B_TX	GPIO3_IO28	FLEXIO2_IO30	LPUART5_RX	CAN2_TX	MQS2_LEFT	JTAG_MUX_TDI			
AC20	R18	USB_B_EN	GPIO2_IO18	FLEXIO1_IO18	LPSPI5_PCS0	LPSPI4_PCS0	TPM5_CH2	MMX_C_DATA09	MMX_D_DATA14	SAI3_RX_BCLK	LEVEL SHIFTER
AC21	N/A	USB_B_OC#									
AC22	B15	USB_B_D_P	USB2_D_P								

3.4. Pin List LCD

Pin List LCD

OSM Pin	MPU Pin	OSM Pin Name	GPIOx / Dedicated Function	Alternative Modes on Pin							Details
				1	2	3	4	5	6	7	
A2	A10	CSI_A_DATA1_N	MIPI_CSI1_D1_N								
A3	B10	CSI_A_DATA1_P	MIPI_CSI1_D1_P								
A4	-	GND	GND								
A5	N/A	CSI_A_DATA2_N									
A6	N/A	CSI_A_DATA2_P									
A7	-	GND	GND								
A8	N/A	USB_C_SSTX_P									
A9	N/A	USB_C_SSTX_N									
A10	-	GND	GND								
A14	N/A	UART_A_RX									
A15	N/A	CH1_RX_N									
A16	N/A	CH1_LINK									
A17	N/A	CH1_TX_N									
A18	N/A	CH0_SYNC_TRIG									
A19	N/A	CH0_RX_N									
A20	N/A	CH0_LINK									
A21	N/A	CH0_TX_N									
A22	F20	UART_C_RX	GPIO1_IO6	LPUART1_CTS_B	LPUART2_RX	LPSPI2_SOUT	TPM1_CH2	SAI1_MCLK			

Pin List LCD

OSM Pin	MPU Pin	OSM Pin Name	GPIOx / Dedicated Function	Alternative Modes on Pin							Details
				1	2	3	4	5	6	7	
B1	B11	CSI_A_DATA0_P	MIPI_CSI1_D0_P								
B2	-	GND	GND								
B3	D10	CSI_A_CLOCK_N	MIPI_CSI1_CLK_N								
B4	E10	CSI_A_CLOCK_P	MIPI_CSI1_CLK_P								
B5	-	GND	GND								
B6	N/A	CSI_A_DATA3_N									
B7	N/A	CSI_A_DATA3_P									
B8	-	GND	GND								
B9	-	GND	GND								
B10	N/A	USB_C_SSRX_P									
B11	N/A	USB_C_SSRX_N									
B13	N/A	UART_A_TX									
B15	N/A	CH1_RX_P									
B16	N/A	CH1_ACT									
B17	N/A	CH1_TX_P									
B18	N/A	CH1_SYNC_TRIG									
B19	N/A	CH0_RX_P									
B20	N/A	CH0_ACT									
B21	N/A	CH0_TX_P									
B22	N/A	Vendor Defined									
B23	F21	UART_C_TX	GPIO1_IO7	LPUART2_TX	LPUART1_RTS_B	LPSPI2_SCK	TPM1_CH3				
C1	A11	CSI_A_DATA0_N	MIPI_CSI1_D0_N								

Pin List LCD

OSM Pin	MPU Pin	OSM Pin Name	GPIOx / Dedicated Function	Alternative Modes on Pin							Details
				1	2	3	4	5	6	7	
C2	Y3	CAM_MCK	GPIO3_IO27	FLEXIO1_IO27	CCM_CLKO2						
C3	N/A	CAM_A_SDA/ CSI_A_TX_N									
C4	N/A	CAM_A_SCL/ CSI_A_TX_P									
C5	-	VCC_6_TEST	VDD_3V3								
C6	Y7	ETH_B_MDC	GPIO4_IO14	FLEXIO2_IO14	LPUART4_DCB_B	SAI2_RX_SYNC	ENET1_MDC (FEC)				
C7	AA6	ETH_B_MDIO	GPIO4_IO15	FLEXIO2_IO15	LPUART4_RIN_B	SAI2_RX_BCLK	ENET1_MDIO (FEC)				
C8	N/A	USB_C_OC#									
C9	N/A	USB_C_VBUS									
C10	N/A	USB_C_EN									
C11	-	GND	GND								
C13	N/A	UART_A_RTS									
C14	N/A	UART_A_CTS									
C15	N/A	CH1_RXC									
C16	N/A	Vendor Defined									
C17	N/A	CH1_TXC									
C18	N/A	TEST_GENERIC									
C19	N/A	CH0_RXC									
C20	R16	SDIO_A_IOPWR	NVCC_SD2								
C21	N/A	CH0_TXC									
C22	N/A	UART_D_RX									
C23	N/A	UART_D_TX									
D1	-	GND	GND								

Pin List LCD

OSM Pin	MPU Pin	OSM Pin Name	GPIOx / Dedicated Function	Alternative Modes on Pin							Details
				1	2	3	4	5	6	7	
D2	N/A	ETH_B_(R)(G)MII_CRS									
D3	-	GPIO_C_0	I2C2_EXP_IO16								
D4	-	GPIO_C_1	I2C2_EXP_IO17								
D5	-	GND	GND								
D6	G21	Vendor Defined	BOOT_MODE[2]	GPIO1_IO11	LPUART2_DTR_B	LPSPI1_PCS0	SAI1_TX_SYNC	SAI1_TX_DATA01	MQS1_LEFT		
D7	H21	Vendor Defined	BOOT_MODE[3]	GPIO1_IO13	LPUART2_RTS_B	LPUART1_DTR_B	LPSPI1_SCK	SAI1_TX_DATA00	CAN1_TX		
D8	-	GND	GND								
D9	N/A	USB_C_ID									
D10	N/A	USB_C_D_P									
D11	N/A	USB_C_D_N									
D13	N/A	UART_B_TX									
D14	N/A	UART_B_RX									
D15	N/A	UART_B_RTS									
D16	N/A	UART_B_CTS									
D17	-	GPIO_A_0	I2C2_EXP_IO00								
D18	-	GND	GND								
D19	-	GPIO_B_0	I2C2_EXP_IO06								
D20	N/A	SDIO_A_WP									
D21	-	SDIO_A_PWR_EN	VSD_3V3								
D22	E20	UART_CON_RX	GPIO1_IO04	LPUART1_RX	LPSPI2_SIN	TPM1_CH0	S400_UART_RX				
D23	E21	UART_CON_TX	GPIO1_IO05	LPUART1_TX	LPSPI2_PCS0	TPM1_CH1	S400_UART_TX				
E1	N/A	ETH_B_(R)(G)MII_COL									

Pin List LCD

OSM Pin	MPU Pin	OSM Pin Name	GPIOx / Dedicated Function	Alternative Modes on Pin							Details
				1	2	3	4	5	6	7	
E2	-	GND	GND								
E3	-	GPIO_C_2/ CAM_B_PWR	I2C2_EXP_IO16								
E4	-	GPIO_C_3/ CAM_B_RST#	I2C2_EXP_IO17								
E15	-	GND	GND								
E16	N/A	ETH_A_(R)(G)MII_ CRS									
E17	-	GPIO_A_1	I2C2_EXP_IO01								
E18	AA2	PWM_0	GPIO3_IO26	FLEXIO1_IO26	CCM_CLKO1						
E19	-	GPIO_B_1	I2C2_EXP_IO07								
E20	Y19	SDIO_A_CMD	GPIO3_IO02	FLEXIO1_IO02	USDHC2_CMD	ENET1_EVENT0_IN (FEC)	CCM_OBSERVE1	I3C2_PUR	I3C2_PUR_B		
E21	-	GND	GND								
F1	U8	ETH_B_(S)(R)(G)MI I_TXD1	GPIO4_IO18	FLEXIO2_IO18	LPUART4_RTS_B	SAI2_RX_DATA02	ENET1_RGMII_TD1 (FEC)				
F2	T10	ETH_B_(S)(R)(G)MI I_TXD3	GPIO4_IO16	FLEXIO2_IO16	SAI2_RX_DATA00	ENET1_RGMII_TD3 (FEC)					
F3	N/A	GPIO_C_4									
F4	N/A	GPIO_C_5									
F15	N/A	ETH_A_(R)(G)MII_ COL									
F16	-	GND	GND								
F17	-	GPIO_A_2	I2C2_EXP_IO02								
F18	R17	PWM_1	GPIO2_IO19	LPSPI5_SIN	LPSPI4_SIN	TPM6_CH2	MMX_D_DATA15	SAI3_RX_SYNC	SAI3_TX_DATA00	PDM_BS03	LEVEL SHIFTER
F19	-	GPIO_B_2	I2C2_EXP_IO8								
F20	-	GND	GND								

Pin List LCD

OSM Pin	MPU Pin	OSM Pin Name	GPIOx / Dedicated Function	Alternative Modes on Pin							Details
				1	2	3	4	5	6	7	
F21	AA19	SDIO_A_CLK	GPIO3_IO01	FLEXIO1_IO01	USDHC2_CLK	ENET_QOS_EVENT0_OUT	CCM_OBSERVE0	I3C2_SDA			
G1	T8	ETH_B_(S)(R)(G)MII_TXD0	GPIO4_IO19	FLEXIO2_IO19	LPUART4_TX	SAI2_RX_DATA03	ENET1_RGMII_TD0 (FEC)				
G2	V8	ETH_B_(S)(R)(G)MII_TXD2	GPIO4_IO17	FLEXIO2_IO17	SAI2_RX_DATA01	ENET1_RGMII_TD2 (FEC)	ENET1_TX_CLK (FEC)				
G3	N/A	GPIO_C_6/ CAM_A_PWR									
G4	N/A	GPIO_C_7/ CAM_A_RST#									
G15	T12	ETH_A_(S)(R)(G)MII_TXD1	GPIO4_IO04	FLEXIO2_IO04	LPUART3_RTS_B	ENET_QOS_RGMII_TD1	I3C2_PUR	I3C2_PUR_B	USB1_OTG_OC		
G16	V12	ETH_A_(S)(R)(G)MII_TXD3	GPIO4_IO02	FLEXIO2_IO02	CAN2_TX	ENET_QOS_RGMII_TD3	USB2_OTG_ID				
G17	-	GPIO_A_3	I2C2_EXP_IO03								
G18	V4	PWM_2	GPIO4_IO29	FLEXIO2_IO29	CCM_CLKO4						
G19	-	GPIO_B_3	I2C2_EXP_IO09								
G20	Y18	SDIO_A_D0	GPIO3_IO03	FLEXIO1_IO03	USDHC2_DATA0	ENET1_EVENT0_OUT (FEC)	CAN2_TX	CCM_OBSERVE2			
G21	AA18	SDIO_A_D1	GPIO3_IO04	FLEXIO1_IO04	USDHC2_DATA1	ENET1_EVENT1_IN (FEC)	CAN2_RX				
H1	U6	ETH_B_(R)(G)MII_TX_CLK	GPIO4_IO21	FLEXIO2_IO21	SAI2_TX_BCLK	ENET1_RGMII_TXC (FEC)	ENET1_TX_ER (FEC)				
H2	-	GND	GND								
H3	W20	RGB_CS#	GPIO2_IO28	FLEXIO1_IO28	LPI2C3_SDA						
H4	-	GND	GND								
H15	W11	ETH_A_(S)(R)(G)MII_TXD0	GPIO4_IO05	FLEXIO2_IO05	LPUART3_TX	ENET_QOS_RGMII_TD0					
H16	U12	ETH_A_(S)(R)(G)MII_TXD2	GPIO4_IO03	FLEXIO2_IO03	ENET_QOS_RGMII_TD2	ENET_QOS_REF_CLK	CAN2_RX	USB2_OTG_OC			
H17	-	GPIO_A_4	I2C2_EXP_IO04								

Pin List LCD

OSM Pin	MPU Pin	OSM Pin Name	GPIOx / Dedicated Function	Alternative Modes on Pin							Details
				1	2	3	4	5	6	7	
H18	N/A	PWM_3									
H19	-	GPIO_B_4	I2C2_EXP_IO10								
H20	Y20	SDIO_A_D2	GPIO3_IO05	FLEXIO1_IO05	USDHC2_DATA2	ENET1_EVENT1_OUT (FEC)	MQS2_RIGHT				
H21	AA20	SDIO_A_D3	GPIO3_IO06	FLEXIO1_IO06	USDHC2_DATA3	MQS2_LEFT	LPTMR2_ALT1				
J1	AA4	ETH_B_(S)(R)(G)MII_RXD0	GPIO4_IO24	FLEXIO2_IO24	LPUART4_RX	SAI2_TX_DATA02	ENET1_RGMII_RD0 (FEC)				
J2	V6	ETH_B_(R)(G)MII_TX_EN(_ER)	GPIO4_IO20	FLEXIO2_IO20	LPUART4_DTR_B	SAI2_TX_SYNC	ENET1_RGMII_TX_CTL (FEC)				
J3	W21	RGB_RESET#	GPIO2_IO27	FLEXIO1_IO27	LPSPI5_PCS1	USDHC3_DATA3	TPM6_CH3	MMX_D_DATA23	CAN2_RX	JTAG_MUX_TMS	
J4	J20	RGB_DE	GPIO2_IO01	FLEXIO1_IO01	LPUART5_RX	LPSPI6_SIN	LPI2C3_SCL	LPI2C5_SCL	MMX_C_DATA00	MMX_D_DE	
J15	U10	ETH_A_(R)(G)MII_TX_CLK	GPIO4_IO07	FLEXIO2_IO07	ENET_QOS_TX_CLK	ENET_QOS_TX_ER					
J16	-	GND	GND								
J17	-	GPIO_A_5	I2C2_EXP_IO05								
J18	N/A	PWM_4									
J19	-	GPIO_B_5	I2C2_EXP_IO11								
J20	-	GND	GND								
J21	Y17	SDIO_A_CD#	GPIO3_IO00	FLEXIO1_IO00	USDHC2_CD_B	ENET_QOS_EVENT0_IN	I3C2_SCL				
K1	Y5	ETH_B_(S)(R)(G)MII_RXD1	GPIO4_IO25	FLEXIO2_IO25	SAI2_TX_DATA03	ENET1_RGMII_RD1 (FEC)	SPDIF_IN				
K2	N/A	ETH_B_(R)(G)MII_RX_ER									
K3	K21	RGB_HSYNC	GPIO2_IO03	FLEXIO1_IO03	LPUART5_RTS_B	LPSPI6_SCK	LPI2C4_SCL	LPI2C6_SCL	MMX_C_HSYNC	MMX_D_HSYNC	
K4	Y21	RGB_DISP	GPIO2_IO29	FLEXIO1_IO29	LPI2C3_SCL						
K15	AA8	ETH_A_(S)(R)(G)MII_RXD0	GPIO4_IO10	FLEXIO2_IO10	LPUART3_RX	ENET_QOS_RGMII_RD0					

Pin List LCD

OSM Pin	MPU Pin	OSM Pin Name	GPIOx / Dedicated Function	Alternative Modes on Pin							Details
				1	2	3	4	5	6	7	
K16	V10	ETH_A_(R)(G)MII_TX_EN(_ER)	GPIO4_IO06	FLEXIO2_IO06	LPUART3_DTR_B	ENET_QOS_RGMII_TX_CTL					
K17	N/A	GPIO_A_6									
K18	N/A	PWM_5									
K19	-	GPIO_B_6	I2C2_EXP_IO12								
K20	N/A	SDIO_B_CLK									
K21	N/A	SDIO_B_CMD									
L1	Y4	ETH_B_(R)(G)MII_RX_DV(_ER)	GPIO4_IO22	FLEXIO2_IO22	LPUART4_DSR_B	SAI2_TX_DATA00	ENET1_RGMII_RX_CTL (FEC)				
L2	-	GND	GND								
L3	K20	RGB_VSYNC	GPIO2_IO02	FLEXIO1_IO02	LPUART5_CTS_B	LPSPI6_SOUT	LPI2C4_SDA	LPI2C6_SDA	MMX_C_VSYNC	MMX_D_VSYNC	
L4	-	GND	GND								
L15	Y9	ETH_A_(S)(R)(G)MII_RXD1	GPIO4_IO11	FLEXIO2_IO11	LPUART3_CTS_B	ENET_QOS_RGMII_RD1	LPTMR2_ALT1				
L16	N/A	ETH_A_(R)(G)MII_RX_ER									
L17	N/A	GPIO_A_7									
L18	-	GND	GND								
L19	-	GPIO_B_7	I2C2_EXP_IO13								
L20	N/A	SDIO_B_D0									
L21	N/A	SDIO_B_D1									
M1	AA5	ETH_B_(R)(G)MII_RXD2	GPIO4_IO26	FLEXIO2_IO26	LPUART4_CTS_B	SAI2_MCLK	ENET1_RGMII_RD2 (FEC)	MQS2_RIGHT			
M2	N/A	ETH_B_SDP	0 = RGMII, 1=RMII (TXCLK and TD2 are connected internally)								PULLDOWN_10K
M3	V21	RGB_B5	GPIO2_IO25	FLEXIO1_IO25	LPSPI7_PCS1	USDHC3_DATA1	TPM4_CH3	MMX_D_DATA21	CAN2_TX	JTAG_MUX_TCK	

Pin List LCD

OSM Pin	MPU Pin	OSM Pin Name	GPIOx / Dedicated Function	Alternative Modes on Pin							Details
				1	2	3	4	5	6	7	
M4	J21	RGB_(PIXEL)CLK	GPIO2_IO00	FLEXIO1_IO00	LPUART5_TX	LPSPI6_PCS0	LPI2C3_SDA	LPI2C5_SDA	MMX_C_CLK	MMX_D_CLK	
M15	Y8	ETH_A_(R)(G)MII_RX_DV(_ER)	GPIO4_IO08	FLEXIO2_IO08	LPUART3_DSR_B	ENET_QOS_RGMII_RX_CTL	USB_OTG_PWR2				
M16	-	GND	GND								
M17	-	ETH_IOPWR	VDD_1V8								
M18	B19	ADC_0	ADC_IN0								
M19	-	VCC_2_TEST2	VDD_SOC_0V85								
M20	-	GND	GND								
M21	V20	SDIO_B_D2	GPIO2_IO26	LPSPI8_PCS1	USDHC3_DATA2	TPM5_CH3	MMX_D_DATA22	SAI3_TX_SYNC	PDM_BS01	JTAG_MUX_TDI	
N1	Y6	ETH_B_(R)(G)MII_RXD3	GPIO4_IO27	FLEXIO2_IO27	ENET1_RGMII_RD3 (FEC)	MQS2_LEFT	SPDIF_OUT	SPDIF_IN			
N2	N/A	RESERVED									
N3	U20	RGB_B3	GPIO2_IO23	FLEXIO1_IO23	USDHC3_CMD	TPM6_CH1	LPI2C5_SCL	SPDIF_OUT	MMX_D_DATA19		
N4	U21	RGB_B4	GPIO2_IO24	FLEXIO1_IO24	LPSPI6_PCS1	USDHC3_DATA0	TPM3_CH3	MMX_D_DATA20	JTAG_MUX_TDO		
N15	AA9	ETH_A_(R)(G)MII_RXD2	GPIO4_IO12	FLEXIO2_IO12	ENET_QOS_RGMII_RD2						
N16	N/A	ETH_A_SDP	0 = RGMII, 1=RMII (TXCLK and TD2 are connected internally)								PULLDOWN_10K
N17	Y1	JTAG_TCK(SWCLK)	GPIO3_IO30	FLEXIO1_IO30	LPUART5_CTS_B	JTAG_MUX_TCK					
N18	A20	ADC_1	ADC_IN1								
N19	W2	JTAG_TMS(SWDIO)	GPIO3_IO29	FLEXIO2_IO31	LPUART5_RTS_B	JTAG_MUX_TMS					
N20	N/A	SDIO_B_D3									
N21	N/A	SDIO_B_D4									
P1	AA3	ETH_B_(R)(G)MII_RX_CLK	GPIO4_IO23	FLEXIO2_IO23	SAI2_TX_DATA01	ENET1_RGMII_RXC (FEC)	ENET1_RX_ER (FEC)				

Pin List LCD

OSM Pin	MPU Pin	OSM Pin Name	GPIOx / Dedicated Function	Alternative Modes on Pin							Details
				1	2	3	4	5	6	7	
P2	-	GND	GND								
P3	U18	RGB_B2	GPIO2_IO22	FLEXIO1_IO22	USDHC3_CLK	TPM5_CH1	TPM6_EXTCLK	LPI2C5_SDA	SPDIF_IN	MMX_D_DATA18	
P4	-	GND	GND								
P15	Y10	ETH_A_(R)(G)MII_RXD3	GPIO4_IO13	FLEXIO2_IO13	ENET_QOS_RGMII_RD3	LPTMR2_ALT3					
P16	N/A	Vendor Defined									
P17	W1	JTAG_TDI	GPIO3_IO28	FLEXIO2_IO30	LPUART5_RX	CAN2_TX	MQS2_LEFT	JTAG_MUX_TDI			
P18	-	GND	GND								
P19	N/A	JTAG_RTCK									
P20	N/A	SDIO_B_D5									
P21	N/A	SDIO_B_D6									
R1	-	GND	GND								
R2	N/A	PCIe_SM_ALERT#									
R3	T21	RGB_B1	GPIO2_IO21	LPSPI4_SCK	LPSPI5_SCK	TPM4_CH1	SAI3_RX_BCLK	SAI3_TX_DATA00	PDM_CLK	MMX_D_DATA17	
R4	T20	RGB_B0	GPIO2_IO20	FLEXIO1_IO20	LPSPI5_SOUT	LPSPI4_SOUT	TPM3_CH1	MMX_D_DATA16	SAI3_RX_DATA00	PDM_BS00	
R15	AA7	ETH_A_(R)(G)MII_RX_CLK	GPIO4_IO09	FLEXIO2_IO09	ENET_QOS_RX_CLK	ENET_QOS_RX_ER					
R16	-	GND	GND								
R17	Y2	JTAG_TDO(SWO)	GPIO3_IO31	FLEXIO1_IO31	LPUART5_TX	CAN2_RX	MQS2_RIGHT	JTAG_MUX_TDO			
R18	F21	BOOT_SEL1#	BOOT_MODE[1]								ONLY FOR FIRST <1ms
R19	N/A	JTAG_nTRST									
R20	-	GND	GND								
R21	N/A	SDIO_B_D7									
T1	N/A	PCIe_SMCLK									

Pin List LCD

OSM Pin	MPU Pin	OSM Pin Name	GPIOx / Dedicated Function	Alternative Modes on Pin							Details
				1	2	3	4	5	6	7	
T2	N/A	PCIe_WAKE#									
T3	R21	RGB_G4	GPIO2_IO16	FLEXIO1_IO16	LPUART3_CTS_B	LPUART4_CTS_B	LPSPI4_PCS2	SAI3_TX_BCLK	PDM_BS02	MMX_D_DATA12	
T4	R20	RGB_G5	GPIO2_IO17	FLEXIO1_IO17	LPUART3_RTS_B	LPUART4_RTS_B	LPSPI4_PCS1	SAI3_MCLK	MMX_C_DATA8	MMX_D_DATA13	
T15	AA10	ETH_MDIO	GPIO4_IO01	FLEXIO2_IO01	LPUART3_RIN_B	ENET_QOS_MDIO	I3C2_SDA	USB_OTG_PWR1			
T16	AA11	ETH_MDC	GPIO4_IO00	FLEXIO2_IO00	LPUART3_DCB_B	ENET_QOS_MDC	I3C2_SCL	USB_OTG_ID1			
T17	N/A	FORCE_RECOVERY#									
T18	N/A	I2S_B_LRCLK									
T19	N/A	I2S_B_BITCLK									
T20	-	SDIO_B_IOPWR	VDD_1V8								
T21	N/A	SDIO_B_CD#									
U1	N/A	PCIe_SMDAT									
U2	-	GND	GND								
U3	P21	RGB_G3	GPIO2_IO15	FLEXIO1_IO15	LPUART3_RX	LPUART8_RTS_B	LPUART4_RX	LPSPI8_SCK	MMX_C_DATA7	MMX_D_DATA11	
U4	-	GND	GND								
U15	V14	SPI_A_SDI_(IO1)	GPIO3_IO23	FLEXIO1_IO23	USDHC3_DATA1	FLEXSPI1_A_DATA01					
U16	V16	SPI_A_SCK	GPIO3_IO20	FLEXIO1_IO20	USDHC3_CLK	FLEXSPI1_A_SCLK					
U17	N/A	RESET_IN#	PMIC_RST_B								PULLUP_100K_NVCC_BBSM_1V8
U18	-	VCC_OUT_IO	NVCC_GPIO								
U19	E21	BOOT_SEL0#	BOOT_MODE[0]								ONLY FOR FIRST <1ms
U20	N/A	SDIO_B_WP									
U21	N/A	SDIO_B_PWR_EN									

Pin List LCD

OSM Pin	MPU Pin	OSM Pin Name	GPIOx / Dedicated Function	Alternative Modes on Pin							Details
				1	2	3	4	5	6	7	
V1	-	GND	GND								
V2	N/A	PCIe_A_PERST#									
V3	N21	RGB_G1	GPIO2_IO13	FLEXIO1_IO13	LPUART8_RX	LPSPI8_SIN	TPM4_CH2	LPI2C8_SCL	PDM_BS03	MMX_D_DATA09	
V4	N/A	RGB_G2	GPIO2_IO14	FLEXIO1_IO14	LPUART3_TX	LPUART8_CTS_B	LPUART4_TX	LPSPI8_SOUT	MMX_C_DATA6	MMX_D_DATA10	
V15	T16	SPI_A_SDO_(IO0)	GPIO3_IO22	FLEXIO1_IO22	USDHC3_DATA0	FLEXSPI1_A_DATA 00					
V16	-	GND	GND								
V17	-	CARRIER_PWR_EN	VDD_1V8								PULLDOWN_10k
V18	U4	I2S_MCLK	GPIO4_IO28	FLEXIO2_IO28	CCM_CLKO3						
V19	N/A	I2S_B_DATA_IN									
V20	-	GND	GND								
V21	H20	I2S_A_DATA_IN	GPIO1_IO14	LPUART2_DSR_B	LPSPI1_SOUT	SAI1_RX_DATA00	SAI1_MCLK	MQS1_RIGHT			
W1	N/A	PCIe_REFCLK_P									
W2	N/A	PCIe_CLKREQ#									
W3	-	GND	GND								
W4	N20	RGB_G0	GPIO2_IO12	SAI3_RX_SYNC	LPUART8_TX	LPSPI8_PCS0	TPM3_CH2	LPI2C8_SDA	PDM_BS02	MMX_D_DATA08	
W15	T14	SPI_A_HOLD_(IO3)	GPIO3_IO25	FLEXIO1_IO25	USDHC3_DATA3	FLEXSPI1_A_DATA 03					
W16	U14	SPI_A_WP_(IO2)	GPIO3_IO24	FLEXIO1_IO24	USDHC3_DATA2	FLEXSPI1_A_DATA 02					
W17	N/A	RTC_PWR									
W18	G21	I2S_A_LRCLK	GPIO1_IO11	LPUART2_DTR_B	LPSPI1_PCS0	SAI1_TX_SYNC	SAI1_TX_DATA01	MQS1_LEFT			
W19	N/A	I2S_B_DATA_OUT									
W20	G20	I2S_A_BITCLK	GPIO1_IO12	LPUART2_CTS_B	LPUART1_DSR_B	LPSPI1_SIN	SAI1_TX_BCLK	CAN1_RX			
W21	H21	I2S_A_DATA_OUT	GPIO1_IO13	LPUART2_RTS_B	LPUART1_DTR_B	LPSPI1_SCK	SAI1_TX_DATA00	CAN1_TX			

Pin List LCD

OSM Pin	MPU Pin	OSM Pin Name	GPIOx / Dedicated Function	Alternative Modes on Pin							Details
				1	2	3	4	5	6	7	
Y1	N/A	PCIe_REFCLK_N									
Y2	-	GND	GND								
Y3	-	VCC_5_TEST	LPD4_VDD2_1V1								
Y4	M21	RGB_R5	GPIO2_IO09	FLEXIO1_IO09	LPUART7_RX	LPSPI3_SIN	TPM3_EXTCLK	MMX_C_DATA03	MMX_D_DATA05	LPI2C7_SCL	
Y5	M20	RGB_R4	GPIO2_IO08	FLEXIO1_IO08	LPUART7_TX	LPSPI3_PCS0	TPM6_CH0	MMX_C_DATA02	MMX_D_DATA04	LPI2C7_SDA	
Y6	L20	RGB_R2	GPIO2_IO06	FLEXIO1_IO06	LPUART6_CTS_B	LPSPI7_SOUT	TPM5_CH0	MMX_D_DATA02	LPI2C7_SDA	PDM_BS01	
Y7	L17	RGB_R0	GPIO2_IO04	FLEXIO1_IO04	LPUART6_TX	LPSPI7_PCS0	TPM3_CH0	MMX_D_DATA00	LPI2C6_SDA		
Y8	-	VCC_IN_5V	VCC_IN_5V								
Y9	-	VCC_IN_5V	VCC_IN_5V								
Y10	-	VCC_IN_5V	VCC_IN_5V								
Y11	-	VCC_IN_5V	VCC_IN_5V								
Y13	N/A	CARRIER_STBY#									
Y14	N/A	RESET_OUT#									
Y15	U16	SPI_A_CS0#	GPIO3_IO21	FLEXIO1_IO21	USDHC3_CMD	FLEXSPI1_A_SS0_B					
Y16	-	VCC_3_TEST	VCC_1V8								
Y17	-	VCC_IN_5V	VCC_IN_5V								
Y18	-	GND	GND								
Y19	N/A	VCC_IN_3V3									
Y20	-	VCC_4_TEST	VDD_ANA_0V8								
Y21	N/A	SPI_B_SCK									
Y22	N/A	SPI_B_SDI									
Y23	N/A	SPI_B_SDO									

Pin List LCD

OSM Pin	MPU Pin	OSM Pin Name	GPIOx / Dedicated Function	Alternative Modes on Pin							Details
				1	2	3	4	5	6	7	
AA1	-	GND	GND								
AA2	N/A	RESERVED									
AA3	N/A	DSI_TE									
AA4	-	GND	GND								
AA5	L21	RGB_R3	GPIO2_IO07	FLEXIO1_IO07	LPUART6_RTS_B	LPSPI3_PCS1	LPSPI7_SCK	MMX_C_DATA01	MMX_D_DATA03	LPI2C7_SCL	
AA6	L18	RGB_R1	GPIO2_IO05	FLEXIO1_IO05	LPUART6_RX	LPSPI7_SIN	TPM4_CH0	MMX_D_DATA01	LPI2C6_SCL	PDM_BS00	
AA7	-	GND	GND								
AA8	-	GND	GND								
AA9	A19	PWR_BTN#	ONOFF								PULLUP_100K_NVCC_BBSM_1V8
AA10	-	GND	GND								
AA11	-	GND	GND								
AA13	N/A	RESERVED									
AA14		GND	GND								
AA15	C20	I2C_A_SCL	GPIO1_IO00	LPUART1_DCB_B	TPM2_CH0	LPI2C1_SCL	I3C1_SCL				PULLUP_2K2_VDD_1V8
AA16	C21	I2C_A_SDA	GPIO1_IO01	LPUART1_RIN_B	TPM2_CH1	LPI2C1_SDA	I3C1_SDA				PULLUP_2K2_VDD_1V8
AA17	-	GND	GND								
AA18	N/A	V_BAT									
AA19	-	GND	GND								
AA20	D20	I2C_B_SCL	GPIO1_IO02	LPUART2_DCB_B	TPM2_CH2	SAI1_RX_SYNC	LPI2C2_SCL	I3C1_PUR	I3C1_PUR_B		PULLUP_2K2_VDD_1V8
AA21	D21	I2C_B_SDA	GPIO1_IO03	LPUART2_RIN_B	TPM2_CH3	SAI1_RX_BCLK	LPI2C2_SDA				PULLUP_2K2_VDD_1V8
AA22	-	GND	GND								

Pin List LCD

OSM Pin	MPU Pin	OSM Pin Name	GPIOx / Dedicated Function	Alternative Modes on Pin							Details
				1	2	3	4	5	6	7	
AA23	L17	SPI_B_CS0#	GPIO2_IO04	FLEXIO1_IO04	LPUART6_TX	LPSPI7_PCS0	TPM3_CH0	MMX_D_DATA00	LPI2C6_SDA		
AB1	N/A	PCIe_A_HSI0_P									
AB2	N/A	PCIe_A_HSI0_N									
AB3	-	GND	GND								
AB4	B9	DSI_DATA3_P/ LVDS_A_LANE3_P	MIPI_DSI1_D3_P								
AB5	A9	DSI_DATA3_N/ LVDS_A_LANE3_N	MIPI_DSI1_D3_N								
AB6	-	GND	GND								
AB7	E6	DSI_CLOCK_P/ LVDS_A_CLK_P	MIPI_DSI1_CLK_P								
AB8	D6	DSI_CLOCK_N/ LVDS_A_CLK_N	MIPI_DSI1_CLK_N								
AB9	-	GND	GND								
AB10	B6	DSI_DATA0_P/ LVDS_A_LANE0_P	MIPI_DSI1_D0_P								
AB11	A6	DSI_DATA0_N/ LVDS_A_LANE0_N	MIPI_DSI1_D0_N								
AB13	A14	USB_A_D_N	USB1_D_N								
AB14	C11	USB_A_ID	USB1_ID								
AB15	-	GND	GND								
AB16	F12	USB_A_VBUS	USB1_VBUS								
AB17	J17	CAN_A_RX	GPIO1_IO09	LPSPI1_PCS1	TPM1_EXTCLK	PDM_BS00	CAN1_RX	MQS1_RIGHT	LPTMR1_ALT2		
AB18	N/A	V_BAT									
AB19	Y2	CAN_B_RX	GPIO3_IO31	FLEXIO1_IO31	LPUART5_TX	CAN2_RX	MQS2_RIGHT	JTAG_MUX_TDO			
AB20	E14	USB_B_VBUS	USB2_VBUS								
AB21	-	GND	GND								

Pin List LCD

OSM Pin	MPU Pin	OSM Pin Name	GPIOx / Dedicated Function	Alternative Modes on Pin							Details
				1	2	3	4	5	6	7	
AB22	E12	USB_B_ID	USB2_ID								
AB23	A15	USB_B_D_N	USB2_D_N								
AC2	N/A	PCIe_A_HSO0_P									
AC3	N/A	PCIe_A_HSO0_N									
AC4	-	GND	GND								
AC5	B8	DSI_DATA2_P/ LVDS_A_LANE2_P	MIPI_DSI1_D2_P								
AC6	A8	DSI_DATA2_N/ LVDS_A_LANE2_N	MIPI_DSI1_D2_N								
AC7	-	GND	GND								
AC8	B7	DSI_DATA1_P/ LVDS_A_LANE1_P	MIPI_DSI1_D1_P								
AC9	A7	DSI_DATA1_N/ LVDS_A_LANE1_N	MIPI_DSI1_D1_N								
AC10	-	GND	GND								
AC14	B14	USB_A_D_P	USB1_D_P								
AC15	N/A	USB_A_OC#									
AC16	N18	USB_A_EN	GPIO2_IO11	FLEXIO1_IO11	LPUART7_RTS_B	LPSPI3_SCK	TPM5_EXTCLK	MMX_C_DATA05	MMC_D_DATA07	LPI2C8_SCL	LEVEL SHIFTER
AC17	G17	CAN_A_TX	GPIO1_IO08	PDM_CLK	CAN1_TX	MQS1_LEFT	LPTMR1_ALT1				
AC18	N/A	DEBUG_EN									
AC19	W1	CAN_B_TX	GPIO3_IO28	FLEXIO2_IO30	LPUART5_RX	CAN2_TX	MQS2_LEFT	JTAG_MUX_TDI			
AC20	R18	USB_B_EN	GPIO2_IO18	FLEXIO1_IO18	LPSPI5_PCS0	LPSPI4_PCS0	TPM5_CH2	MMX_C_DATA09	MMX_D_DATA14	SAI3_RX_BCLK	LEVEL SHIFTER
AC21	N/A	USB_B_OC#									
AC22	B15	USB_B_D_P	USB2_D_P								

3.5. Power Supply

> The byteENGINE can be powered with 3.3V to 5.5V.
> The recommended power supply is 5V.

PCA9451AHN Power Manage IC (PMIC) for i.MX93

3.6. Boot Modes byteENGINE IMX9x

The OSM Standard implements two BOOT Pins: BOOT_SEL0# and BOOT_SEL1#

The iMX9x has four Bootpins:

Bootmode Pin	IMX9x PAD	OSM PAD	Note
BOOT_MODE0	UART1_TXD	(U19) BOOT_SEL0#	automatically disconnected after Boot
BOOT_MODE1	UART2_TXD	(R18) BOOT_SEL1#	automatically disconnected after Boot
BOOT_MODE2	SAI1_TXFS	(D6) Vendor Defined	disconnect logic needed on baseboard
BOOT_MODE3	SAI1_TXD0	(D7) Vendor Defined	disconnect logic needed on baseboard

BOOT_MODE2 and BOOT_MODE3 are connected to Vendor Defined Pins.
While BOOT_MODE0 and BOOT_MODE1 are automatically disconnected on the byteENGINE after power on reset, the logic for BOOT_MODE2 and BOOT_MODE3 must be handled on the baseboard separately. The boot sequence can be redefined with OTP writing.

CPU	BOOD_MODE (3:0)	BOOT Source
Cortex-A55	0000	Boot from internal Fuses
	0001	Serial Download (USB1)
	0010	USDHC1 8-bit eMMC 5.1
	0011	USDHC2 4-bit SD 3.0
	0100	FlexSPI Serial NOR
	0101	FlexSPI Serial NAND 2K
Cortex-M33	1000	LPB: Boot From Internal Fuses
	1001	LPB: Serial Downloader (USB1)
	1010	LPB: USDHC1 8-bit 1.8V eMMC 5.1
	1011	LPB: USDHC2 4-bit SD 3.0
	1100	LPB: FlexSPI Serial NOR
	1101	LPB: FlexSPI Serial NAND 2K

See the Datsheets of NXP for more Details: NXP i.MX 9

4. Ordering info

The Order Code allows customers to easily recognize the detailed specification of the ordered SOM. Please refer to chapter Decision guidance byteENGINE IMX9x for further information.

byteENGINE-IMX9[TYPE]-[SPEED]-[RAM]-[FLASH]-[variant]-[temp-range]-[revision]

[TYPE]	**CPU type**	Comprehensive, details see Additional Information
[SPEED]	**Clock speed**	800 MHz / 900MHz / 1400 MHz / 1700 MHz
[RAM]	**RAM size**	512 / 768 / 1024 / 1536 / 2048 MB
[FLASH]	**eMMC flash size**	8 / 16 / 32 / 64 / 128 GB
[variant]	**Module population Variant**	[O] OSM-ext [L] LCD
[temp-range]	**Temperature range**	[C] Consumer 0° to +70° C [I] Industrial -40°C to +85 °C
[revision]	**Revision**	2.1

5. References

Notice

Files can only be downloaded with login credentials. Please request your download credentials via support@bytesatwork.ch or contact your sales representative

Links

- Schematic of the connector OSM-S Variant OSM-ext:
  Schematic of the connector OSM-S Variant OSM-ext
- Schematic of the connector OSM-S Variant LCD:
  Schematic of the connector OSM-S Variant LCD
- Altium Sheet of the connector OSM-S Variant OSM-ext:
  Altium Sheet of the connector OSM-S Variant OSM-ext
- Altium Sheet of the connector OSM-S Variant LCD:
  Altium Sheet of the connector OSM-S Variant LCD
- Altium Library:
  Altium Library
- STEP Model:
  STEP Model
- Detailed Pinout for byteENGINE IMX9x:
  Detailed Pinout of byteENGINE IMX9x
- NXP i.MX 9 Family:
  NXP i.MX 9
- i.MX9 Config Tool:
  i.MX Config Tool
- bytesatwork on github:
  https://github.com/bytesatwork
- byteWIKI:
  https://bytewiki.readthedocs.io/en/latest/som/imx93_osm.html

bytesatwork

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Help

bytewiki.readthedocs.io